

NEW JERSEY PAINT-SKIP TECHNICAL MANUAL

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1. INTRODUCTION

NEW JERSEY

Snowplowable Raised Pavement Markers (SRPMs) have been installed on the center lines and edge lines, in line with the skip lines and in gore areas on various New Jersey roadways. This action was taken as a result of the guidelines developed over many years of testing and development.

The effect of the SRPMs at nighttime (especially during rain) is to provide delineation that would otherwise be lost to the driver, and is a vast improvement over newly painted lane lines. During daytime hours the driver cannot use the SRPMs for guidance and therefore lane lines are required. Both SRPMs and lane lines are required for twenty-four hour, all-weather guidance.

During the many years of testing and development of SRPMs in New Jersey the SRPMs were placed only near the lines. When SRPMs were adopted for use throughout the State, they were placed upon the painted lines thus presenting a consistent roadway to the motorists day and night. This placement required instrumentation to prevent painting the reflectors in the metal castings of SRPMs when the lane lines were restriped.

Various options were considered. Commercially obtained off-the-shelf instrumentation was not available. Development of instrumentation by the State was considered. The time required was excessive and the cost exceeded desirable limits. It was decided to obtain instrumentation through an agreement with the original inventor of the Paint-Skip unit for the Ohio Department of Transportation since this was the only instrumentation that worked on the magnetic principle.

The original agreement required manufacturing six Paint-Skip units, their installation on three striping trucks (two units per truck, one per paint gun carriage), making the units operational, the acceptance of the units through trials on roadway sections, a six month warranty after acceptance, and the composition of a technical manual for the construction, operation and repair of the units.

During the course of this agreement a more versatile Paint-Skip unit was developed which was offered to and accepted by the State. The agreement was modified to include delivery of another five units. All striping trucks in the New Jersey Department of Transportation were then equipped with two of the revised Paint-Skip units each. A spare unit was also available.

The agreement required that a technical manual be

written and that the technical manual contain the theory of operation, construction procedures, troubleshooting procedures, test points with waveforms, voltage and current values, schematic diagrams, assembly drawings, the required test equipment and tools, replaceable parts list, list of parts sources, operational procedures, calibration procedures, installation and acceptance procedures, and all other instructions relating to the maintenance and repair of the units.

This manual is the result of the above requirement.

The New Jersey Department of Transportation now requires in its bid specification that all new striping trucks be delivered with Paint-Skip or equivalent units already installed and that they be operational. The accuracy of the Paint-Skip units or their equivalent shall be such that, with proper control settings, on a properly maintained striper and roadway, and in the absence of other metal than SRPMs on or in the roadway (reinforcing bars too near the surface, foil-backed pavement marking tape, bridge expansion joints, etc.), only one reflector or less in 10,000 will be painted when at least one-half the width of the SRPM is within the width of the antenna.

OHIO (Author)

This operation and service manual was prepared under an agreement (as amended) between the author and the New Jersey Department of Transportation for production, delivery and acceptance testing of eleven Paint-Skip units.

Paint-Skip is a device which is attached to a traffic paint striper to prevent its painting over (and destroying the reflectivity of the reflector in) snowplowable, raised pavement markers. Paint-Skip was invented by the author in 1977 at the Ohio Department of Transportation. Ohio was then in the process of developing specifications for all aspects of the use of snowplowable, raised pavement markers (then nicknamed "Life-Lites" in Ohio but abbreviated "SRPM" herein, according to New Jersey's custom), and the need was foreseen for some arrangement to avoid painting over the reflectors.

The first Paint-Skip design was distance-based, making use of a fifth-wheel. A project interim report (Reference 1)* was published, which describes the first design. A second design was completed in 1978. It was time-based and about half as costly, because of the elimination of the fifth-wheel. Like the first model, it acted through

* References are listed on page 13.

the "host" paint controller and required electrical interface with the host. Thirteen of these Paint-Skips were made for the Ohio Department of Transportation, and a few more are being used by striping contractors. A report (Reference 2) was published in 1978 which included construction and operation information. The design is therefore in the public domain. The report is available from the Ohio Department of Transportation. It was this second design which was originally the subject of the agreement between the author and the New Jersey Department of Transportation.

In 1981 the author was commissioned by Traffic Specialists, Inc. of Springboro, Ohio to design a version of Paint-Skip which would not require electrical interface with the host controller, but instead act through auxiliary electric air valves on the signal air controlling the paint guns. Such a device, furnished with auxiliary air valves and other hardware, could be sold over-the-counter for the user to install.

This (third) version of Paint-Skip was in use when, in March, 1982, the author, with the agreement of Traffic Specialists, Inc., proposed to the New Jersey Department of Transportation that it be substituted for the second design Paint-Skip. The proposal was accepted and the units were delivered and accepted.

In accordance with the agreement, the departments of Highways or of Transportation of the State of New Jersey and of all the other states, and the United States Department of Transportation, are granted "non exclusive, non transferable and royalty free license to practice each invention and to manufacture, use and dispose of any article or material and to use any method that may be developed as a part of the work under this Agreement."

Manufacture and use of this device under all other circumstances shall be in accord with the rights of ownership of the design accruing to Mr. Mark Barton, MB Enterprises, P.O. Box 4205, Newark, Ohio 43055 (telephone number 614-345-6197), who acquired all interest in the design from Traffic Specialists, Inc., and who currently is marketing the device.

The author gratefully acknowledges the most gracious and unstinting help of the contract manager, Mr. Karl Brodtman of the Division of Research and Demonstration, New Jersey Department of Transportation.

NOTES: THIS IS A TECHNICAL MANUAL. ALL FIGURES AND ALL WAVEFORMS ARE GROUPED TOGETHER IN THE APPENDICES FOR EASE AND CONVENIENCE OF PERSONS WHO HAVE TO MAKE USE OF THE MANUAL FOR THE INSTALLATION, ADJUSTMENT, MAINTENANCE AND TROUBLESHOOTING OF THE PAINT-SKIP UNITS.

ELEVEN PAINT-SKIP UNITS WERE FURNISHED UNDER THE REFERENCED CONTRACT. THESE ARE CONSECUTIVELY NUMBERED BEGINNING WITH SERIAL NUMBER 101 AND ENDING WITH NUMBER 111. THIS MANUAL UNLESS OTHERWISE DESIGNATED APPLIES ONLY TO THOSE ELEVEN UNITS.

2. THEORY OF OPERATION

GENERAL

Paint-Skip causes the paint to stop for a short space around each SRPM. A typical paint system is shown schematically in Figure 1. (All figures are found in numerical order in Appendix A.) The system consists of a pressurized paint tank, usually a paint heater, a paint gun, and control system. The host (existing) control system consists of the host paint controller (used by the operator to select the line patterns) which electrically controls a host air valve which in turn controls signal air to turn on and off the paint gun. A fifth wheel, or odometer system, supplies distance information for the host controller. In a Paint-Skip installation an auxiliary air valve is placed between the host air valve and the paint gun. The Paint-Skip control box, receiving signals from the antenna when a metal SRPM passes under it, electrically controls the auxiliary air valve, which overrides the host air valve to shut off the paint in the presence of an SRPM. Not shown are minor systems such as atomizing air at the paint gun nozzle; bead tanks, lines, guns; and so forth. These are not directly related to the Paint-Skip operation.

HOST PAINT SYSTEM

Most stripers are equipped with paint guns that use an air pressure signal to control paint flow. Paint (or other material) is present in the gun, under pressure. A spring-closed valve controls the flow of paint. This valve is opened by the signal air pressure acting against a piston or diaphragm in the gun which is connected to the paint valve. Atomizing air is led to the paint nozzle to produce the characteristic "fan" of paint. When the signal air is shut off and exhausted, the paint valve closes under the action of the return spring, and paint stops.

The signal air is controlled by an electrically operated air valve having three ports, called "IN"; "OUT" (or "CYL", for "cylinder"); and "EXH" (for "exhaust"). In the "open" position air under pressure at the input port is led to the output port (and from there to the paint gun) and at the same time the third, or exhaust, port is closed. The paint gun is turned on.

In the "closed" position the input port is closed and the output port is led to the exhaust port. The air pressure holding the paint gun valve open is exhausted and

paint stops.

The air valve can be made "normally open" so that the electric signal closes it, or "normally closed" so that the electric signal opens it.

The electric current flows through a solenoid (coil) in the valve and the valve elements are moved by magnetic forces due to this current. When current is shut off suddenly, as in normal operation, a voltage of opposite polarity to that first impressed on the solenoid is induced in the solenoid by the collapsing magnetic field. This rapidly-rising "spike" is a troublesome or harmful noise to the electronic paint control system, including Paint-Skip. A common remedy is to place a rectifier diode across the solenoid with its cathode at the terminal that is made positive by the controller. The voltage-reversed spike is shorted by the diode. The resulting current in the solenoid causes a small delay in the valve action.

There is another, potentially more serious, source of delay. When the signal air is exhausted to stop painting, the air in the paint gun and the hose connecting the gun and air valve must pass to the atmosphere through an orifice in the valve. If the hose is long, or the orifice too small (a 1/4-inch orifice is the norm, but occasionally 1/8-inch ones are found), paint shut-off will be delayed.

To override the host air valves and cause the paint to stop for a short space around each SRPM with a minimum of disruption to the existing equipment, normally-open, electric air valves are placed in the signal air lines between each paint gun and its respective control valve. These auxilliary valves are wired in parallel and closed by short current pulses from Paint-Skip as an SRPM passes under the guns. These normally-open auxilliary air valves can be left in place but electrically disconnected from Paint-Skip and the striper will function normally.

The placement of auxilliary valves close to the paint guns can also lower gun response time. In this position the connecting air lines are short and the gun turn-off is faster because less signal air needs to be exhausted.

PAINT-SKIP (Refer to Figure 2)

Paint-Skip consists of a small box containing electronic circuits and the controls regulating their operation, an antenna-sensor which is mounted just above the road and in front of the paint guns, and the auxilliary air valves with associated hardware. The specified auxilliary valves have 1/4-inch orifices.

The antenna is part of a "mine detector" circuit which responds to the metal SRPM by triggering a timing circuit

which produces two sequential time intervals. The end of the first timing interval triggers the second timing interval, and at the end of the second interval Paint-Skip resets to be ready for another SRPM.

The first timing interval delays paint shut-off until the guns are close to the SRPM. The second interval actuates the auxilliary air valves and shuts off paint as the guns pass over the SRPM. Both intervals are adjustable over a wide range. The first interval is called "DELAY". A control of that name is on the control panel of Paint-Skip. There is also a fine adjustment on the control panel for this interval, called "SPEED COMP". Because Paint-Skip is based on time, not distance, proper operation depends on a fairly constant truck speed. SPEED COMP (speed compensator) is intended for use by the operator to compensate for slight speed variations, to keep the skip centered on the SRPMs longitudinally.

The duration of the second time interval, and the length of the skip, are adjusted by means of the "SKIP" control.

Bead guns, because of their slow response to on and off commands, are not controlled by Paint-Skip.

The relationships among the various system delays and the two timing intervals of Paint-Skip are discussed below.

*Let T_1 be the first timing interval of Paint-Skip, and T_2 the second interval. Then

$$T_1 = ((D - S/2) / V) - T(\text{off})$$

$$\text{and } T_2 = (S / V) - T(\text{on}) + T(\text{off})$$

where D = distance between leading edge of sensor antenna and paint guns

S = length of skip in paint over the SRPM, centered on the reflector of the SRPM

V = truck speed, or painting speed

$T(\text{off})$ = delay between electrical "off" command and cessation of painting

$T(\text{on})$ = delay between electrical "on" command and beginning of painting.

Solving the first equation for V ,

$$V = (D - S/2) / (T_1 + T(\text{off})).$$

It can be seen that painting speed, V , is increased by increasing D and by lowering T_1 and $T(\text{off})$. In practice,

T(off) is usually the major effect, reaching values of 0.15 second or greater in some cases (corresponding to 21 inches at 8 miles/hour). Therefore D will be made as large as possible and T1 will be made close to zero to maximize speed. For well-maintained installations in which proper auxilliary valves are used, MOUNTED CLOSE TO THE PAINT GUNS, skipping speeds of fifteen miles/hour have been achieved.

A mid-range setting of the SPEED COMP control is used at the normal painting speed so that the operator will be able to compensate for changes in speed. The DELAY control is advanced (turned clockwise) to enable lower painting speeds.

A typical system with a conservative skip length, S, of about one foot will tolerate truck speed variations of plus or minus about 1.5 miles/hour without painting the reflector, and the operator's use of the SPEED COMP control will increase the tolerance to plus or minus about three miles/hour. Experienced crews will tend to shorten S to about nine inches for an excellent line appearance.

Solving the second equation for skip length, S,

$$S=V(T(\text{on})+T2-T(\text{off})).$$

The dependence of S on V is immediately apparent. The main point, however, is the system's dependence on the delays T(on) and T(off). As these are in turn dependent on consistent paint gun performance, GOOD MAINTENANCE OF THE GUNS AND ASSOCIATED EQUIPMENT IS OF GREAT IMPORTANCE.

Paint-Skip is triggered by a metallic object moving through the high frequency (about 480 kHz) magnetic field around the antenna sensor, which is part of an oscillator circuit. Foil-backed pavement marking tape, reinforcing bars close to the pavement surface, manhole covers, etc., will be detected about as well as SRPMs. The metal causes an increase in inductance of the antenna, and the Paint-Skip oscillator's frequency undergoes a rapid rise-fall cycle as the antenna passes over the SRPM. Slow changes (drift) in the oscillator frequency will not cause a skip reaction. Sensitivity is controlled by a combination of antenna height above the pavement and the setting of the sensitivity (SENS) front-panel control. This control requires a special adjustment procedure, described in the "Operation and Maintenance" section of this manual.

The on-off switch and rear-panel jack for attachment of a manual skip control complete the operator's controls.

It will inevitably be asked, why an odometer-based device was not built, to be independent of painting speed. In fact, the first Paint-Skip, described in a 1977 interim report of the Ohio Department of Transportation (Reference 1), was such a device. Its parts cost was about double that of the final design because of the cost of the fifth-wheel for distance sensing. The paint system delays

(notably T(off)), however, made the distance settings meaningless at any acceptable painting speed (eight-plus miles/hour); and there was still the undesirable variation in skip position over the marker with changes in painting speed. Rather than take the expensive step of modifying the paint system for very fast response, and to save the cost of the distance measuring components, a time-based Paint-Skip was designed, the forerunner of the unit described herein. That unit was described in a 1978 report of the Ohio Department of Transportation (Reference 2).

CIRCUIT DETAILS (Refer to Figure 3)

Inductor L1 is the antenna sensor; when connected to the "Antenna" jack, J1, it becomes part of the oscillator circuit around transistor Q1, consisting of Q1, L1, R1-R3, and C1-C3. The oscillation frequency is about 475 kHz.

Capacitor C4 couples the sampled frequency to the phase-lock loop (PLL) circuit around Z1. (See Reference 3.) Diodes D1 and D2 protect the Z1 input from excessive voltage swings. The PLL consists of a voltage-controlled oscillator (VCO), a phase comparator, and a loop filter consisting of R5, R9 and C5. The VCO is made to track the incoming signal in phase. Phase errors are sensed by the phase comparator, which issues voltage pulses (smoothed by the loop filter) to raise or lower the control voltage which, in turn, raises or lowers the frequency of the VCO to restore the phase match between the VCO and the input signal. The control voltage is sampled at pin 10 of Z1.

As an SRPM passes under the antenna, temporarily increasing its inductance, the Q1 oscillator frequency undergoes a rise-fall cycle. The PLL follows the input frequency as it maintains a zero-phase difference between its VCO and the input signal. The VCO control voltage therefore also undergoes a rise-fall cycle, which is superimposed on the steady-state DC level. A SRPM will typically cause a momentary rise in the VCO frequency of one or two kHz. The corresponding rise in voltage at pin 10 of Z1 is 13 to 26 millivolts. Thirteen millivolts per kHz can be said to be the "demodulation gain" of the system.

Components C5, R5 and R6 establish the range of operation of the PLL at about 200 to 700 kHz. Moderately out-of-tolerance components around Q1 and Z1 will not move the oscillator frequency out of the PLL operation range.

Z2, an operational amplifier, is used as a "tracking" comparator with hysteresis. It "tracks", in that slow voltage changes at pin 10 of Z1 (due to temperature effects on circuit components, moisture or paint absorption by the antenna or road surface, etc.) will not trigger the comparator because of the AC coupling (by C9) of the Z2

inverting input (pin 2) to ground. Triggering describes the reaction of the comparator to small voltage increases at the non-inverting input compared with the inverting input (pin 3). This voltage is amplified by the circuit by such a large factor that practically any positive voltage between pins 3(+) and 2(-) of Z2 results in the pin 6 output going to V+; otherwise the output goes to ground. Slow voltage changes at pin 3 will charge C9 through R11 and pin 2 will "track" pin 3, although obviously not perfectly. Rapid changes will trigger Z2 because C9 prevents effective tracking at high rates of change. Hysteresis refers to the positive feedback from pin 6 to pin 3 through R12, which results in an upper trigger point below which a rising input voltage (pin 3 positive with respect to pin 2) will not drive the output positive (V+), and a lower trigger point above which a falling input voltage will not drive the output negative (ground). The upper trigger point is higher than the lower trigger point, and the difference is called hysteresis. The effect is to make the comparator resistant to input noise, which in this case includes the slight input voltage that is present when the input increases slowly for reasons given above. Another feature of this comparator circuit is the use of the input offset adjustment, R13, marked "SENS" (sensitivity) on the front panel, to force a slightly negative effective input offset voltage between pins 3 and 2.

If the input rise-fall pulse to pin 3 of Z2 is rapid enough and of sufficient amplitude, the output will undergo a rapid rise from zero volts (ground) to V+, and then return to zero. This pulse starts the Paint-Skip timing sequence. It can be seen why PAINT-SKIP WILL RESPOND TO RELATIVE MOTION BETWEEN METAL OBJECTS AND THE ANTENNA BUT NOT TO SUSTAINED PRESENCE OF SUCH AN OBJECT. IN FACT, AN SRPM CAN BE LAID ON THE ANTENNA AND PAINT-SKIP WILL STILL OPERATE.

The practical setting of the SENS control is slightly counterclockwise of the setting where the inherent input offset voltage of Z2 is exactly nulled, and the circuit oscillates. Further negative offset (control counterclockwise) lowers the sensitivity of Paint-Skip to metal objects by requiring greater and greater input pulse levels to trigger Z2. THIS, WITH THE ANTENNA HEIGHT ADJUSTMENT, CAN OFTEN BE USED TO DISCRIMINATE BETWEEN SRPMs AND METAL TAPE, REINFORCING BARS, ETC.

Given the variations in input offset voltages from part to part among Z2 samples, the physical threshold setting of the SENS control will vary from box to box. Use of A- or B-suffix parts for Z2 will minimize this effect, but at added cost.

The output pulse from Z2 is used to trigger the dual one-shot timer, Z3. The circuit is configured for positive-trigger, non-retriggerable operation, and the first

section triggers the second section at the completion of its output pulse. (See the product description reproduced in Appendix D of this manual for details.)

Duration of the first interval is set by front-panel controls DELAY and SPEED COMP. The duration, T1, is given approximately by

$$T1=C12(R16+R17+R18),$$

where capacitance is in Farads
resistance is in Ohms
time is in seconds.

The range of T1 is from practically zero to about 0.75 second. Because operators will tend to run with T1 at a minimum to gain painting speed, and because the circuit will latch "on" if $R16+R17+R18=0$, R16 establishes a negligible minimum of about 0.005 second for T1 to ensure triggering of T2. Whatever the DELAY setting, it is intended that normal painting speed be established with SPEED COMP at mid range, giving the operator the ability to compensate for plus and minus truck speed variations.

Duration of T2 is given approximately by

$$T2=(C13)(R19)$$

No minimum is established for T2, and it will latch "on" if R19 is set to zero. The range is from practically zero to about 0.5 second.

C19 and R24 are used to hold the Z3 reset terminals momentarily at ground upon turn-on of Paint-Skip. This prevents any Z3 output from causing an unwanted paint skip. It does result, however, in about a 3/4-second period of "warm-up" before Paint-Skip will react to SRPMs.

The output of Z3 is buffered by Z4d and Z4c to drive Q2, a PNP Darlington power transistor. There is an alternate mounting position shown for R21 to enable normally-on operation of Q2 if, for example, only normally-closed auxilliary air valves are available. Since Q2 operates from the battery voltage and the buffer output logic-1 level is about eight volts (V+), Zener diode D3 is used to prevent a logic-1 buffer output from turning on Q2. R21 limits base drive current. Diodes D4 and D5 limit the reverse voltage spike from the auxilliary valve(s) to about 16 volts to protect Q2. Use of D5 to allow the spike to rise to 16 volts speeds valve action because reverse current does not flow in the valve solenoid(s) for as long a time as it would with just D4 across the solenoid(s). As noted earlier, current due to the shorted reverse voltage "spike" acts to hold the valve closed, the same as current flowing in the normal direction.

Light emitting diodes M1, M2 and M3 are driven by

sections of inverting buffer Z4 through current-limiting resistors. The signal for driving M1 comes from pin 1 of Z1. This signal consists of negative-going pulses (from V+ to ground) coinciding with the rising edge of the 480 kHz VCO waveform, whose widths are proportional to the phase error between the input and VCO output. Therefore when the VCO is "out of lock" with the input, the resulting wide pulses at pin 1 will cause M1 to light. Because very short pulses are present even when the PLL is "in lock", C18 is needed to prevent a slight glow in M1 during normal operation. A GLOWING M1 ALMOST ALWAYS INDICATES A PROBLEM WITH THE ANTENNA, L1, OR ITS CONNECTOR.

"Raw" 12-volt power is conditioned by the filter composed of C21, L2 and C22; Zener diode D6 (for both overvoltage and reversed-polarity protection); 8-volt regulator Z5; and capacitors C15 and C17. Note that the PLL, Z1, is decoupled by R4 and C6. This circuit is very sensitive to supply voltage noise. C20 and C21 are placed at the point of entry of 12-volt power, right at connector P2, to shunt very high frequency noise components to ground. Part of the bench checkout procedure is to touch the leads of an air valve solenoid to the power leads of Paint-Skip lightly enough to produce sparks. The bursts of high-frequency noise which result must be successfully attenuated, so that Paint-Skip does not trigger falsely. Regulator Z5 produces a nominal 8-volt output so long as the supply is greater than the output by at least two volts. Conservatively, Paint-Skip must have at least 10.5 volts input to satisfy this requirement. Abnormally-high or reversed-polarity inputs will cause the 1/2-ampere fuse to open, because of Zener diode D6.

Zener diode D7 supplies the anodes of the light emitting diodes. It is used to prevent logic-1 buffer outputs from turning on the light emitting diodes.

Manual actuation of Paint-Skip can be accomplished if desired by making up a remote switch as shown in the schematic. When plugged into the rear panel "REM" (remote) jack, J3, closure of the switch will turn on Q2 and stop painting. D8, D9 and R23 protect the circuit from harmful signals that may be introduced at J3.

Connectors P2 and J2 enable enough flexibility that Q2 can, if desired, be powered from a separate 12-volt circuit, for instance in the case of an electrically operated paint gun.

Provision was also made for a "Test-Run-Defeat" switch at R15 as shown on the schematic. Moving the switch to the "Test" position would trigger a skip sequence. Grounding R15 ("Defeat") would prevent skipping. This function is normally performed by just using the on-off switch, S1.

3. REFERENCES

1. RICHARDSON, W.C., PAINT-SKIP (INTERIM REPORT), BUREAU OF TRAFFIC, OHIO DEPARTMENT OF TRANSPORTATION, NOVEMBER, 1977.
2. RICHARDSON, W.C., PAINT-SKIP (FINAL REPORT), BUREAU OF TRAFFIC, OHIO DEPARTMENT OF TRANSPORTATION, MARCH, 1978.
3. "THE RCA COS/MOS PHASE-LOCKED LOOP...A VERSATILE BUILDING BLOCK FOR MICRO-POWER DIGITAL AND ANALOG APPLICATIONS", APPLICATION NOTE ICAN-6101, RCA CORPORATION.

4. CONSTRUCTION

Construction of Paint-Skip should be undertaken only by persons with previous experience in electronic fabrication. No attempt is made here, for instance, to detail the preparation of art work for making printed circuits, or to instruct the technician in how to strip wire or solder correctly. These and other skills can only be learned with practice. Parts procurement should be complete before the work is started. Substitutions of equivalent or better parts for those shown in the Parts List can be made with confidence. In most cases suggested substitutes are listed.

Mark, punch and drill the lower half of enclosure M6 using full size templates in Figures 4, 5, and 6. Be careful to correctly differentiate between the front and rear panels. Deburr all holes, degrease and apply rub-on letters M28 according to Figures 7 and 8. (All parts are identified in the parts list in Appendix B.) Apply at least three coats of protective finish M29 over the letters.

Refer to Figure 9, the chassis parts layout, in which parts orientation and terminal nomenclature are shown, for the following steps:

1. Disassemble J2 (78RS8). Install P2 (86-CP8) in the flange in place of the jack and secure with the clip. This assembly will be called P2; the socket will become J2. Align so that the polarizing ridge will be as shown in Figure 9. Assemble to chassis using two each M23a,b,c.
2. Assemble J1 to chassis using two each M23a,b,c.
3. Assemble J3 to chassis so that the wire lug "T" (tip connection) is uppermost.
4. Install terminal strip M21 using two each M23d,f and three M23e. Use one lockwasher between lug 1 and the chassis.
5. Be sure the area under Q2 is deburred and smooth. Install Q2 using insulator kit M24 and one each M15 and M23c. Spread the leads of Q2 so that they enter lugs 4,5 and 6 of M21. The step washer and nylon screw enter from outside the chassis. Coat the mica insulator with heat conductive grease M38. The rectangular spacer goes between the nut and the tab of Q2. Tighten so that the screw is slightly stretched, squeezing out excess grease. BE AWARE THAT A STEP WASHER THAT HAS TOO LONG A SLEEVE CAN PREVENT SNUGGING THE TRANSISTOR UP TO THE CHASSIS. TEST EACH STEP WASHER, AND SHORTEN THE SLEEVE WITH SANDPAPER IF NECESSARY.

6. Install fuseholders M4 and M5 as shown. Rubber washers go outside the chassis.
7. Install threaded standoffs M16,17,18 and 19 using one each M23a,b for each standoff. The lockwashers go between the standoffs and chassis.
8. Install potentiometers R13,17,18 and 19 using the lockwashers furnished with them inside the chassis. (Read step 12 and return here.) Use flatwashers M23g under the nuts outside the chassis. Install the clutch nuts of R13,18 and 19 finger tight.
9. Install terminal strip M8 using two each M23a,c and three M23b. One lockwasher goes between lug 8 and the chassis.
10. Install light emitting diodes M1,M2 and M3 using attaching hardware M30a,b,c. Orient as shown. Cathode leads (K) have shoulders.
11. Install switch S1.
12. Fasten knob M14 to R17. If the 53C1 part was substituted for R13, the shaft will have to be cut off. Support the shaft in a vise while cutting.

Using Figure 10 as a guide, "stuff" the printed circuit board (PCB). Observe polarity markings on capacitors where shown. Integrated circuit sockets are installed with the notched end corresponding with pin 1. Looking at the component side of the PCB with the large solder pads for off-board wires to the left, all integrated circuit sockets will have their notched ends (pin 1) to the left. Keep all components tight to the PCB. Jumpers are made using clippings from the diodes D4-D7. Carefully examine all solder joints for integrity, cold ("frosty"-looking) joints or bridging. Use only high quality solder such as that listed as M7.

Proceed to the Wiring List for chassis wiring and follow all instructions therein. Note that parts are called out by their Parts List designators. "NS" means "no solder" (connect only). "S1", "S2", etc. mean to solder a particular connection, where the numeral confirms the number of conductors that join at that place. The entire assembly should be carefully examined at the end of construction. Check for proper connections, good solder joints and correct positions of the parts. Finally, bundle the chassis wires into a "harness" using string ties or other methods.

WIRING LIST

1. SOLDER Q2 LEADS (M21-4,5,6) (RIVET ENDS OF TABS) AND TRIM FLUSH WITH TERMINAL STRIP.
2. PLACE C18 BETWEEN M3 "ANT" LED CATHODE K (M8-7) (NS) AND GROUND LUG (M8-8) (S1)
3. INSTALL LEDS (M1,M2,M3) AND BEND LEADS DOWN INTO LARGE HOLES IN TERMINALS OF M8 (NS). CATHODES K (SEE FIGURE) GO TO M8-3,5,7.
4. PUT 5/16" PIECE OF 1/8" SHRINK TUBE M33 OVER M21-8 (GROUND LUG)
5. JUMPER P2-5(S1) AND P2-6(S1). USE INSULATED WIRE. STRIP 3/4" OF INSULATION OFF EACH END OF JUMPER. . . . 2 1/2"
6. PUT C22 IN RIVET ENDS OF TABS OF M21-1(GND) (S1) AND M21-2(S1). C22 IS ABOVE M21. TRIM LEADS FLUSH WITH M21.
7. PUT 1 1/2" PIECE OF 1/2" SHRINK TUBE M32 OVER CHOKE L2.
8. PUT CHOKE L2 BETWEEN M21-2(NS) AND M21-7(NS). CHOKE SHOULD HANG 3/16" BELOW M21. USE SPAGHETTI M22 ON LEADS.
9. INSERT (NS) C20 BETWEEN P2-1 AND P2-7. INSERT (NS) C21 BETWEEN P2-2 AND P2-7. TWO CAPACITOR LEADS WILL BE IN P2-7. PUSH CAPACITORS IN AS CLOSE AS POSSIBLE TO P2.
10. CONNECT (USING INSULATED WIRE) P2-7(S3) TO GROUND LUG M21-1(NS) 3"
11. GROUND LUG M21-1(NS) TO SLEEVE TERMINAL "S" OF J3(S1). . . . 2"
12. COLLECTOR C OF Q2(NS) TO P2-3(S1). 5 1/2"
13. CHOKE L2 (M21-7) (S2) TO OUTER FUSE (1/2 AMP) OUTER LUG (S1) 3 1/2"
14. CHOKE L2 (M21-2) (S2) TO POWER SWITCH S1 LOWER INSIDE TERMINAL (S1). 9 1/4"
15. INNER FUSE (5 AMP) OUTER CONNECTION (S1) TO POWER SWITCH S1 LOWER OUTSIDE TERMINAL (S1). 6 1/2"
16. INNER FUSE CENTER LUG (S1) TO P2-2(S2) 8 1/4"
17. OUTER FUSE CENTER LUG (S1) TO P2-1(S2) 8 1/4"
18. POWER SWITCH S1 CENTER OUTSIDE TERMINAL (S1) TO EMITTER E OF Q2 (S1). 8 1/2"
19. MARK BOTH ENDS OF "ANT GND" LEAD ON PCB (PRINTED CIRCUIT BOARD) WITH WHITE PAINT. BE SURE THAT MARK IS AWAY FROM END SO THAT STRIPPER DOES NOT REMOVE IT. TWIST "ANT ~" AND "ANT GND" LEADS ON PCB TOGETHER. CONNECT "ANT ~" LEAD TO TIP TERMINAL (S1) OF J1. CONNECT "ANT GND" LEAD TO GROUND TERMINAL (S1) OF J1 2X(2 3/4")

20. "A SENS" ON PCB TO R13-CCW (S1) 10 3/4"
21. "B SENS" ON PCB TO R13-CW (S1) 8 3/4"
22. "T1" ON PCB TO R17-CCW (S1). 5"
23. "T2" ON PCB TO R19-W (S1). 7 3/4"
24. NO CONNECTION TO "DEFEAT" ON PCB.
25. "REMOTE SW." ON PCB TO TIP "T" TERMINAL OF J3 (S1) 8"
26. "DET" ON PCB TO CATHODE K OF M1 "DET" LED (M8-3)(S2) . 6 1/4"
27. "ANT" ON PCB TO CATHODE K OF M3 "ANT" LED (M8-7)(S3) 8 1/4"
28. "SKIP" ON PCB TO CATHODE K OF M2 "SKIP" LED (M8-5)(S2) 7 1/4"
29. "VLED" ON PCB TO ANODE A OF M1 "DET" LED (M8-2)(NS). . 5 3/4"
30. USING INSULATED WIRE, JOIN ALL LED ANODES A
(M8-2,4,6)(S3,S2,S2) 2X(1 1/4")
31. "+12 V" ON PCB TO POWER SWITCH S1 CENTER INSIDE
TERMINAL (S1). THIS IS ROUTED AROUND THE BACK OF
THE BOX 16"
32. "VDD" ON PCB TO R18-W (NS) 6"
33. R18-W (S2) TO R19-CCW (S1) 2 1/4"
34. "GND" ON PCB TO GROUND LUG M21-1 (NS). 8"
35. "C" ON PCB TO COLLECTOR C OF Q2 (S2) 9"
36. "B" ON PCB TO BASE B OF Q2 (S1) 9 1/2"
37. GROUND LUG M21-1 (S4) TO R13-W (S) 12"
38. R17-W (S) TO R18-CCW (S) 2 3/4"
39. WIRE J2. THE HALF OF THE PLUG SET P4-J4 WITH RED LEAD
COMING FROM AN INSULATED TERMINAL GOES TO J2 AND WILL
BE CALLED P4. THE OTHER HALF WITH RED LEAD COMING
FROM A BARE TERMINAL WILL BE CALLED J4.
 - A. PUSH BOTH LEADS OF P4 THROUGH STRAIN-RELIEF CAP OF J2.
 - B. TRIM BOTH LEADS FROM P4 TO SAME LENGTH AND STRIP.
 - C. RED LEAD FROM P4 TO J2-3(S). USE 1/2" PIECE OF 1/8"
SHRINK TUBE ON THE CONNECTION.
 - D. WHITE LEAD FROM P4 TO J2-5(S). USE 1/2" PIECE OF 1/8"
SHRINK TUBE ON THE CONNECTION.
 - E. 19" PIECE OF 16-GA. RED WIRE TO J2-1(S) AND J2-2(S)
 - F. 19" PIECE OF 16-GA. BLACK WIRE TO J2-6(S) AND J2-7(S)
 - G. PUSH BOTH 16-GA. WIRES THROUGH THE STRAIN-RELIEF CAP OF
J2 AND INSTALL CAP ON J2.
40. CLEAN FLUX FROM PCB AND INSTALL PCB ON STANDOFFS.
41. TRIM WIRE ENDS THAT PROTRUDE FROM THE PINS OF P2.
42. INSERT FUSES AND INTEGRATED CIRCUITS AND TEST UNIT.

NOTE: YOU MAY PREFER TO CUT PCB WIRE LEADS TO LENGTH AND SOLDER THEM TO THE PCB IMMEDIATELY AFTER STUFFING THE BOARD, THEN DEFLUX. HERE IS A SUMMARY OF THE WIRE LEADS AND LENGTHS. LEAVE THE OUTBOARD ENDS UNSTRIPPED UNTIL READY TO CONNECT.

PCB PAD NAME	WIRE LENGTH
A SENS	10 3/4 INCHES
ANT ~	2 3/4
ANT GND	2 3/4 (MARKED WHITE BOTH ENDS)
B SENS	8 3/4
T1	5
T2	7 3/4
DEFEAT	N/C
REMOTE SW	8
DET	6 1/4
ANT	8 1/4
SKIP	7 1/4
VLED	5 3/4
+12V	16
VDD	6
GND	8
C (COLLECTOR)	9
B (BASE)	9 1/2

Construct the antenna sensor, L1. The antenna is made from a seventeen-inch piece of clear, straight 2x6 plank according to Figure 12. A router is used to remove wood for the figure-eight wire slot. Magnet wire or another type of 14 AWG wire is wound around the two "islands", seven turns each in the same sense (direction). Splice, solder and insulate the coil and cable M31. Tie a knot in the cable close to the splice. The coil, splice and knot are potted (cemented) into the slot using the same epoxy that is used to install SRPMs (M35).

The wire coils should be as compact as possible in section (turns close to each other) and as close to the bottom of the slot as possible. Do not abuse the wire prior to potting, as shorts between turns will ruin the antenna. Pegs or some other devices should be used to hold the wire down while the glue sets.

The cable assignment is shown in Figure 12. The white (clear) insulated wire is alone and goes to the tip of plug P1. Black and shield (drain wire) go to the shell (ground) of P1.

When complete, the antenna and 17 feet of cable have the following properties (all are approximate):

Resistance	0.45 ohm
Inductance	35 microHenries
Q	0.55

The frequency of oscillation of a typical antenna and Paint-Skip will be around 475 kHz. The antenna should be held away from metal objects for the test.

Before installing Paint-Skip, perform the checkout operations given in the section "Checkout and Troubleshooting."

5. INSTALLATION

There are only six critical points to installing Paint-Skip:

1. The 12-volt power furnished to the Paint-Skip controller must be between 10.5 and 14.5 volts and must be free of electrical "noise."
2. The control box must be kept out of the rain.
3. The antenna must be mounted securely so that it does not vibrate or swing or interfere with existing truck or paint carriage components.
4. The antenna must be thirty inches or more ahead of the paint guns.
5. The antenna wire must be protected.
6. Air lines connecting auxilliary air valves and paint guns should not be over 24 inches long.

Install the antenna at least thirty inches in front of, and centered on, the paint guns. It should be positioned so that the long sides are at right angles to the direction of travel, and must traverse with the guns. Attachment should be rigid enough to prevent vibration of the antenna, and the antenna should be clear of metal mud guards, wheels (including paint carriage caster wheels in the forward-pointing or reversed direction), frames, metal-clad hoses, etc., which could be sensed and cause spurious skips. Carriages that tend to bob around, perhaps because of an undamped caster wheel oscillation, must be stabilized, because excessive vertical bobbing of the antenna will cause detection failures and painted SRPMs. Attachment will vary with the truck and preferences of the mechanic. Welded or bolted-on support brackets are equally good. Typically, two steel angle brackets are attached securely to the paint carriage, pointing forward. The material will be steel, 1 1/2 or 2 inch webs of 1/4 inch thickness. The brackets will support the antenna at least 30 inches ahead of the guns. The forward ends of the brackets will be spread apart and drilled to accept two 1/2 to 5/8 inch diameter all-thread rods, 9 inches on centers. The antenna will be drilled in the area of the "islands" inside the potted coils, to accept the all-thread rods 9 inches on centers (although that distance may vary). The all-thread rods are long enough to allow adjustment of the antenna road clearance from one to four inches. The rods are attached to the antenna using two nuts and two flatwashers. The rod on the bottom of the antenna is left protruding from the lower nut just enough to peen over. The lower nut is backed down into the peening and the nut above is run down hard to secure the antenna. The

rods are held to the brackets with nuts above and below the brackets, allowing height adjustment. The antenna wire must be taped to the supports to protect it from chafing or tearing out. RUN THE WIRE TO THE PAINT-SKIP CONTROLLER VIA A PROTECTED ROUTE.

Install the auxilliary air valves M39, with M40 and M41 in the paint gun signal air lines, between the host air valves and the guns. Mount them as close as possible to the paint guns. They may in some cases be close nipped to the guns. Put the filters in the EXH ports to exclude dirt. Pipe the CYL port to the paint guns, and the IN ports to the CYL (output) ports of the host air valves, using 1/4 inch ID hose. Check to see that the host air valves and lines have 1/4 inch orifices or larger, and replace them if necessary. Action of the normally-open auxilliary valves will be adversely affected if there is upstream flow restriction. This effect will cause the auxilliary valves to seem to leak from the EXH ports on host turn-on. Sufficient pressure and flow will prevent this.

Wire all auxilliary air valves in parallel and connect to the Paint-Skip polarized valve connector, J4. Polarity is unimportant. Use 16 AWG automotive primary wire (M36 and/or M37) and protect it from damaging conditions. It is always best to solder wire connections. Do not use acid core solder. Use of splicing devices of the type that employ insulation displacing forks in a hinged plastic snap-together shell is discouraged.

Run power supply lines from the Paint-Skip main connector to a source of noise-free 12 volt power. Use 16 AWG automotive primary wire (M36 and M37) and solder all splices. Run the lines to either the chassis or compressor engine area. The black lead coming out of the Paint-Skip main connector strain relief is ground, the red one is positive. The 12 volt source may be switched by an ignition or other switch, but may not share a fused circuit with any other device. Paint-Skip is internally fused, but the user may also fuse the line at the source with a five ampere fuse. With a voltmeter, verify that the black Paint-Skip supply wire is ground and the other is +11 to +14 volts with the engine running. All power connections shall be clean, secure, soldered and insulated.

NOTE: In extreme cases, some electrical devices in the existing system may cause spurious skips. Devices with solenoids (valves, counters, etc.) or devices which draw enough current to momentarily lower the voltage at Paint-Skip to 10.5 volts or less may cause this condition. Solenoids can be suppressed for "back-EMF" using a rectifier diode (see the THEORY section of this manual for details). Extreme voltage loss can usually be traced to shorted devices or bad (resistive) connections.

Attach the Paint-Skip control box to a clean, convenient place out of the weather. Do not drill the box for attaching screws, except that the top may be drilled in the left and right ends if it is first removed from the bottom. Any fasteners used must not contact interior components, and must be fastened to the top so that they do not loosen and fall inside. Provision must be made for easy detachment in case of need to move the box out of the rain.

Note that auxilliary air valves are wired to the 2-wire polarized plug set P4-J4 attached to the main connector J2. By acquiring additional valves, antenna and polarized plugs, users can quickly change from left to right side operation of Paint-Skip simply by changing antenna and auxilliary valve connections and re-adjusting the SENS control. If Paint-Skip is to be used on both sides of the truck at the same time, a second control box is required.

6. OPERATION AND MAINTENANCE

First, review the operation of the controls and indicators.

FRONT PANEL

1. "DELAY" This rotary control sets the delay (T1) timing circuit between zero and about 1/2 second, to adjust for the distance between the antenna and paint guns, the speed of the striper and the response time of the paint guns. Maximum striping speed with Paint-Skip will be at the "zero" (counterclockwise) setting.
 2. "SPEED COMP" (speed compensator) This rotary control (with pointer knob) is a fine adjustment of the delay (T1) timer. If normal striping speed is established with the pointer at the "twelve o'clock" position, then the paint operator can use it to compensate for speed changes of about plus or minus 1.5 miles/hour.
 3. "SKIP" This rotary control sets the length of the "skip" (T2) timer and therefore the length of the skip over the SRPM. Skip length is also dependent on striping speed.
 4. "SENS" (Sensitivity) This rotary control adjusts the sensitivity of the SRPM sensing circuit.
- NOTE: DO NOT OVER-TIGHTEN THE CLUTCH NUTS ON THE ROTARY CONTROLS. FINGER-TIGHT IS USUALLY ENOUGH TO PREVENT ACCIDENTAL TURNING OF THE SHAFTS.
5. "ON-OFF" This toggle switch controls the operation of Paint-Skip. It can be used to momentarily disable Paint-Skip to avoid skipping for manhole covers, etc. There is a one second "warm-up" upon turn-on, during which Paint-Skip will not respond.
 6. "DET" (Detection) This LED indicator indicates the detection of a SRPM and the beginning of the delay (T1) timer. Its duration is not adjustable and is not important.
 7. "SKIP" This LED indicator lights during the skip (T2) interval.
 8. "ANT" (Antenna) THIS LED INDICATOR LIGHTS IF THERE IS A MALFUNCTION IN THE SENSOR CIRCUIT.

BACK PANEL

9. Fuse holders. Use only the indicated amperage fuses.
10. "REM SW" (Remote Switch) A normally-open switch, wired to a 1/8 inch mini plug inserted here, can be used to skip manually. Plug and switch are not furnished.
11. "MAIN" This 8-pin connector is disconnected when the control box is stored. It should be protected from dirt and paint.
12. "ANT" (Antenna) The SRPM sensor antenna is plugged in here. Protect the plug from dirt and paint, and keep it tight-fitting to the jack, to avoid loose connections and undesirable "extra" skips.

ADJUSTMENT

It is assumed that the Paint-Skip was bench tested successfully, and that the installation was correctly performed. Proceed as follows. Failure at any step should lead the user to the sections on installation and troubleshooting.

1. Double check all connections and be sure that battery voltage is present at Paint-Skip.
2. ADJUST THE ANTENNA TO A HEIGHT ABOVE THE PAVEMENT OF TWO TO THREE INCHES.
3. Set SPEED COMP, DELAY and SKIP fully clockwise.
4. Turn on Paint-Skip power switch.
5. Adjust SENS control about five degrees counterclockwise of the point where spontaneous DET indicator flashing occurs. All three indicators should remain dark.
6. Slide a metal plate such as a license plate or 4x6 inch aluminum plate under the antenna. This must be done briskly. The DET indicator should blink, then the SKIP indicator should light for about one half second after a 3/4 second pause. At the same time, the auxilliary air valve(s) should be heard to respond.

7. Prepare for a test run by laying out some approximately 4x6 inch metal plates in a path easily followed by the striper, about twenty feet apart. The plates may be steel or aluminum. Lay the plates perpendicular to the direction of painting. Set SPEED COMP at mid range and DELAY fully counterclockwise. Set SKIP at mid range. Re-check the setting of the SENS control.

8. Make a painting run over the metal plates at eight miles/hour, watching for detections at each plate and rotating the SKIP control until a ten or twelve inch skip is achieved. Pay no attention to whether or not the plates are painted.

9. Leaving the control settings as-is, make another run over the plates, varying the speed until the skips are centered over the plates. This is the maximum speed for the existing hardware configuration, with SPEED COMP centered to allow operator compensation for speed variation. SKIP may have to be readjusted to restore the desired skip length for the speed.

10. If the speed is too fast then advance the DELAY control slightly and repeat the run until satisfied.

11. SPEED COMP will enable the operator to compensate for plus or minus variations in painting speed. Experiment until its operation is familiar. If the truck slows, the skip will fall behind the SRPM. Turning the SPEED COMP control clockwise will advance the skip. If the truck speeds up, the skip will move ahead of the SRPM. Turning the SPEED COMP counterclockwise will move the skip to the rear.

If reinforcing bars, metal foil pavement marking tape, etc. cause spurious skips, the SENS control or the antenna height can be varied in an attempt to correct the situation, although it is not always possible to achieve this. Try lowering the antenna as far as possible and reducing the SENS setting (counterclockwise). The SENS adjustment will be much more critical in this situation, and the chance is increased that some SRPMs will be painted. This may nevertheless be preferable to the spurious skips that result from the causes mentioned. Foil tape has been especially troublesome for Paint-Skip because it remains on the pavement for years. It can affect Paint-Skip operation even where the foil is worn through by traffic at the high points, and the color is worn off, so that it can hardly be seen by the striper operator. Some authorities have been persuaded to discontinue use of metal foil in favor of Paint-Skip operations.

During long periods of not being used, the Paint-Skip controller and antenna should be disconnected and stored. Do not allow the controller to become wet.

MAINTENANCE

Paint gun hygiene is the most important maintenance item for successful Paint-Skip operation. Gun action must be as rapid as possible. More frequent flushings and overhauls should be expected.

The gun signal air system, including the auxilliary air valves, also needs care. Take care that hoses are not pinched, that exhaust port mufflers are clean, and that the regulated air pressure is correct.

Check the condition of the antenna wire and keep it from being damaged. If it becomes damaged, splice with soldered and insulated connections. Keep the antenna plug and jack clean and tight.

The paint carriage must move smoothly. Maintain proper tire pressure and correct any tendency for caster wheels to oscillate.

7. CHECKOUT AND TROUBLESHOOTING

EQUIPMENT NEEDED

1. A ten or fifteen MHz bandwidth or greater triggered oscilloscope, dual trace, 10 mV/division sensitivity or greater, for example:
 - a. Leader Model LBO-514
 - b. B&K Model 1420P (battery portable)
 - c. B&K Model 1476P
 - d. Tektronics Model T922
 - e. Phillips Model PM3207
2. A digital multimeter with 0.5% basic DC accuracy, 3 1/2 digit, with milliampere ranges, for example:
 - a. Fluke Model 8020B
 - b. Data Precision Model 945
3. A frequency counter is desirable but not necessary, for example Fluke Model 1900A.
4. Any lab power supply, continuously variable DC from 0 to 25 volts at 2 amps, for example B&K Model 1601.
5. Two spare auxilliary air valves, M39.
6. A spare Paint-Skip antenna.
7. Recommended stock of spare parts (see PARTS LIST).
8. Tools
 - a. Soldering iron of 30 or fewer watts, with 3-wire (grounded) cord.
 - b. Wick type desoldering aid.
 - c. Integrated circuit puller, for example General Cement #41-614.
 - d. Integrated circuit test clip, for example General Cement #9487.
 - e. Miscellaneous hand tools: long-nose pliers, screwdrivers, diagonal wire cutters, etc.

Voltages and waveforms are measured between circuit points cited and chassis ground. (Waveform pictorials are given in Appendix C.) Care must be exercised to avoid shorting adjacent electrodes when using test probes. Follow operation and safety instructions of the manufacturers of the test instruments used. CMOS integrated circuits are susceptible to damage due to static electricity discharge.

Precautions are prescribed in any CMOS handbook/catalog.

In making repairs, use only a grounded (3-wire) soldering iron of not over 30 watts. To remove parts, the use of a wick-type desoldering device is recommended. Do not overheat or the printed circuit and component may be damaged. On finishing, remove solder flux with any of several solvents, taking care not to contaminate integrated circuit socket contacts. Integrated circuits must not be removed or replaced with power applied to the circuit.

BENCH CHECKOUT

Connect the Paint-Skip to the power supply, plug in the antenna, adjust SENS according to step 5 of the ADJUSTMENT section and connect one of the spare auxilliary air valves to polarized connector P4. Set SPEED COMP to mid-range, DELAY to zero, and SKIP to mid-range. Perform the following tests:

CAUTION: NEVER APPLY MORE THAN 20 VDC TO PAINT-SKIP POWER INPUT TERMINALS.

Test 1 Voltage Regulation

Connect the multimeter (set to measure 0 to 20 volts DC) between the + end of C15 and chassis ground. Turn on the power supply and adjust the output to seven volts. Slowly increase the supply voltage while observing the voltmeter. When the voltage at C15 stops rising (at about 8.0 volts) stop and note the supply voltage. The supply voltage minus the regulated voltage must be less than 2.5 volts, and the regulated voltage must be 8 volts plus or minus 10%.

Test 2 Input Current

With 13.0 volts input measure the current in one of the power conductors at J2 using the multimeter as a milliammeter in series with the conductor. Use a scale to read 0 to 100 milliamperes. The input current must be 23 plus or minus 5 milliamperes.

Test 3 Oscillator

Connect one channel of the oscilloscope between the center terminal of J1 and chassis ground. The vertical amplifier should be set for 2 volts/division and the sweep should be set at 1 microsecond/division. The probe is assumed to be 1:1, or having no attenuation. The waveform should look like the one shown in Waveform 1: about 16 volts

peak to peak, and about 4.8 cycles in 10 microseconds, or 480 kHz. The values obtained must be within 10% of these. A frequency counter may be used instead of the oscilloscope for all but the voltage measurement.

Test 4 Basic Operation

With the antenna suspended, tease the antenna (pass a metal plate briskly under it) and observe that the auxilliary valve is actuated (it clicks).

Test 5 REM SW Function

Using a jumper wire, momentarily connect the "T" and "S" terminals of the REM SW jack J3. The air valve should actuate.

Test 6 LED Operation

Short the antenna center terminal of J1 to chassis ground. The ANT LED M1 should light. Unplug the antenna. M1 should again light. Plug in the antenna. Tease the antenna again. The indicator LEDs M2 and M3 should light in sequence. (The valve will actuate while M3 is lighted.)

Test 7 Control Range

Turn SPEED COMP and DELAY fully counterclockwise. Turn SKIP fully clockwise and tease the antenna. The valve should actuate for about 1/2 second the instant the antenna is teased. Turn SKIP nearly fully counterclockwise (about 9:00 position). The valve should make a very short click when the antenna is teased. (If the SKIP control is reduced too far the valve will not respond even though a current pulse is delivered. Minimum valve time is about 0.02 second.) Place SKIP at mid-rotation. Turn SPEED COMP to full clockwise position. A noticeable delay should exist between teasing the antenna (the DET LED flashes) and the valve sound. Turn DELAY fully clockwise. There should be a 3/4 second delay before the valve actuates. Note the position of the SENS control. It should be at mid-range plus or minus 45 degrees when in adjustment.

Test 8 Transistor Q2 Saturation Voltage

Turn SKIP fully counterclockwise and tease the antenna. The valve should lock on. Using the voltmeter measure the voltage to ground at either terminal of the 5 ampere fuse holder M12 and at the collector of Q2. The difference must not be more than 0.9 volts. A nominal value is 0.8 volt.

Test 9 Noise Immunity

With Paint-Skip powered, touch the leads of the second spare auxilliary valve repeatedly to the power input terminals at the ends of the wires coming from J2. Paint-Skip should not trigger falsely because of the

electrical noise produced.

TEST FAILURE PROCEDURES

Follow the indicated procedure(s) in case one or more of the above Tests fail. Check by part substitution unless otherwise instructed. Each test procedure is based on the success of the previous one.

- 1 a. If the output voltage V+ does not rise with the supply voltage to 8 VDC, then using the voltmeter trace the voltages from the input (J2 pin 1) through M11, L2, S1 and Z5. One of these components may have failed "open"; or one of the capacitors C21, C22, C17 or C15; or Z5 or diode D6 may be shorted.
b. If V+ tracks the input voltage up to and beyond 8.8 VDC then Z5 should be replaced.
- 2 Excessive current indicates a short to ground in P2/J2, Z5, L2, D6, C21, C22, C17 or C15.
- 3 Be sure that P1/J1 are clean and tight. Try a known good antenna. Be sure V+ is present, then substitute Q1, C2, C3, C4, R1-R3, D1, D2.
- 4 Check setting of SENS control. Check fuse M12. Check all chassis wiring connections. Check printed circuit for incorrect insertion of parts and bad or bridged solder joints. If these checks are negative, then isolate faulty section by connecting oscilloscope to read Waveforms 7,8,9 and 10. Make connections of the probes as specified on the respective Waveform. If Waveform 7 is not correct, then suspect (substitute) Z1 and Z2 and associated components. If Waveform 8 is not correct then suspect Z2 and Z3 and associated components. If Waveform 9 is not correct then suspect Z3 and associated components. If Waveform 10 is not correct then suspect Z3, Z4c, Z4d, R21, D3, Q2, D4, D5, S1 and M12.
- 5 Check wiring of J3.
- 6 If just one LED is not lighting, then replace it. Substitute Z4 and D7.
- 7 Check chassis wiring of all rotary controls.
 - a. (no response to SPEED COMP or DELAY or SKIP)
Substitute Z3; check C12, C13.

- b. (no response to SPEED COMP or DELAY) Substitute R17, R18, C12.
 - c. (no response to SKIP) Substitute R19, C13.
 - d. (SENS not centered plus or minus 45 degrees) Substitute Z2. Use A-suffix part.
- 8 Observe Waveform 10. Z3 (pin 9) should behave as shown. Check M12, S1, D3, R21, Z4d, Z4c, D4, D5 and Q2.
- 9 Check C15, C17, C20, C21, C22, L2, Z5. Be sure that C20 and C21 are pushed close to P2 so that their leads are as short as possible.

VOLTAGE AND WAVEFORM TABLE

Voltages DC (VDC) or waveforms are indicated for most terminals of the transistors and integrated circuits. Waveforms referred to are pictured in Appendix C. For these tests the controls are set as follows:

SPEED COMP--mid range
 DELAY-----fully counterclockwise
 SKIP-----mid range.

The supply voltage is nominally 12.5 VDC. V+ is nominally 8.0 VDC.

Q1 collector	Waveform 1
base	Waveform 2
emitter	Waveform 3
Q2 collector	0 VDC
base	+12.5 VDC (supply voltage)
emitter	+12.5 VDC/Waveform 10 during skip cycle
Z1 pin 1	Waveform 5
5	0
6	Waveform 6
7	Waveform 6
8	0
9	3.6 VDC
10	1.8 VDC/Waveform 7
11	1.7 VDC
12	5.6 VDC
14	Waveform 4
16	7.6 VDC

Z2 pin 1 0.07 VDC
 2 2.2 VDC
 3 1.8 VDC
 4 0
 5 0.07 VDC
 6 0
 7 V+
 8 7.6 VDC

Z3 pin 1 0
 2 7.9 VDC (*)
 3 7.4 VDC (**)
 4 0
 5 V+
 7 V+
 8 0
 9 V+
 10 0
 11 0
 12 V+
 13 7.9 VDC (*)
 14 7.6 VDC (***)
 15 0
 16 V+

* V+ through R24 loaded by the meter input impedance

** Depends on settings of R17, R18

*** Depends on setting of R19

Z4 pin 1 V+
 2 Waveform 5
 3 inverted Waveform 5
 4 V+
 5 0
 6 V+
 7 0
 8 0
 9 V+
 10 0
 11 0
 12 V+
 14 Waveform 5
 15 inverted Waveform 5

Z5 input terminal +12.5 (supply voltage)
 output terminal V+ (8.0 VDC)
 ground terminal 0

TROUBLESHOOTING GUIDE

1. No response from Paint-Skip, no power to control box
 - a. blown fuse in control box or at source
 - b. broken or shorted power leads
 - c. 12 volt supply polarity reversed
 - d. control box defective (perform BENCH CHECKOUT)

2. DET and SKIP LEDs light but Paint-Skip auxilliary valves are dead
 - a. blown 5 amp fuse in control box
 - b. polarized connector P4/J4 defective or pulled apart
 - c. broken or shorted wires to Paint-Skip aux. valves
 - d. valve exhaust port screens plugged with dirt
 - e. defective valve

3. Spurious skips, no apparent cause
 - a. loose or dirty antenna plug and jack P1/J1
 - b. wire broken in antenna plug P1
 - c. SENS control out of adjustment
 - d. antenna wire pinched or abraded, open or shorted
 - e. electrical noise on 12 volt supply
 - f. metal object moving close to antenna, e.g. caster wheel of paint carriage, mud guard
 - g. low voltage on 12 volt supply
 - h. defective antenna
 - i. other metal objects in road, e.g. aluminum foil pavement marking tape, reinforcing bars, etc.
 - j. defective control box (perform BENCH CHECKOUT, step 9)

4. ANT LED indicator blinks or glows steadily
 - a. loose or dirty antenna plug and jack P1/J1
 - b. wire broken in antenna plug P1
 - c. SENS control out of adjustment
 - d. antenna wire pinched or abraded, open or shorted
 - e. metal object moving close to antenna, e.g. caster wheel of paint carriage, mud guard
 - f. defective antenna

5. Unable to detect SRPMs (DET indicator either lights continuously or does not blink when SRPM passes under sensor; ANT light is dark)
 - a. SENS control out of adjustment
 - b. antenna adjusted too high above highway
 - c. defective antenna
 - d. defective Paint-Skip controller (perform BENCH CHECKOUT)

6. Skip length and/or position varies, truck speed constant
 - a. defective SPEED COMP, DELAY or SKIP control
 - b. broken or shorted aux. valve wires

- c. defective valves
 - d. plugged screens in Paint-Skip aux. air valve exhaust ports
7. Indistinct or unequal leading or trailing edges of paint lines during either normal operation or skipping; or noticeably delayed turn-on (not skipping)
- a. sluggish paint guns (overhaul guns)
 - b. open or shorted wires to Paint-Skip aux. valves
 - c. plugged screens in Paint-Skip aux. valve exhaust ports
 - d. sluggish or defective aux. air valves
 - e. existing system air valves or hoses with restricted air passages
 - f. low air pressure
 - g. incorrect host system air valves with smaller than 1/4 inch orifices

NOTE: Causes of unequal performance of paint guns can be traced by selecting "double yellow" pattern and making a paint run over metal plates (see ADJUSTMENT). Switch the signal air lines to the paint guns. If the error remains the same in the paint pattern, then the gun(s) are at fault.

8. An unwanted skip is produced on turn-on
- a. On units with serial #107 or above, perform BENCH CHECKOUT. Locate cause of slower than normal rise in V+ at turn-on, which momentarily pulls the base of Q2 low enough to turn it on and cause a short skip.
 - b. On units with serial numbers under #107, change components R24, C6 and C15 to the values specified in the PARTS LIST. These parts were changed at #107 to prevent the turn-on skip, which manifested itself in but one unit.
9. ANT indicator LED glows slightly, all else normal
- a. On units with serial #107 and above, replace Z1.
 - b. On units with serial number below #107, add C18 between lugs 7 and 8 of terminal strip M8.

APPENDIX A

FIGURES

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FIGURE 1

PAINT SYSTEM OPERATION

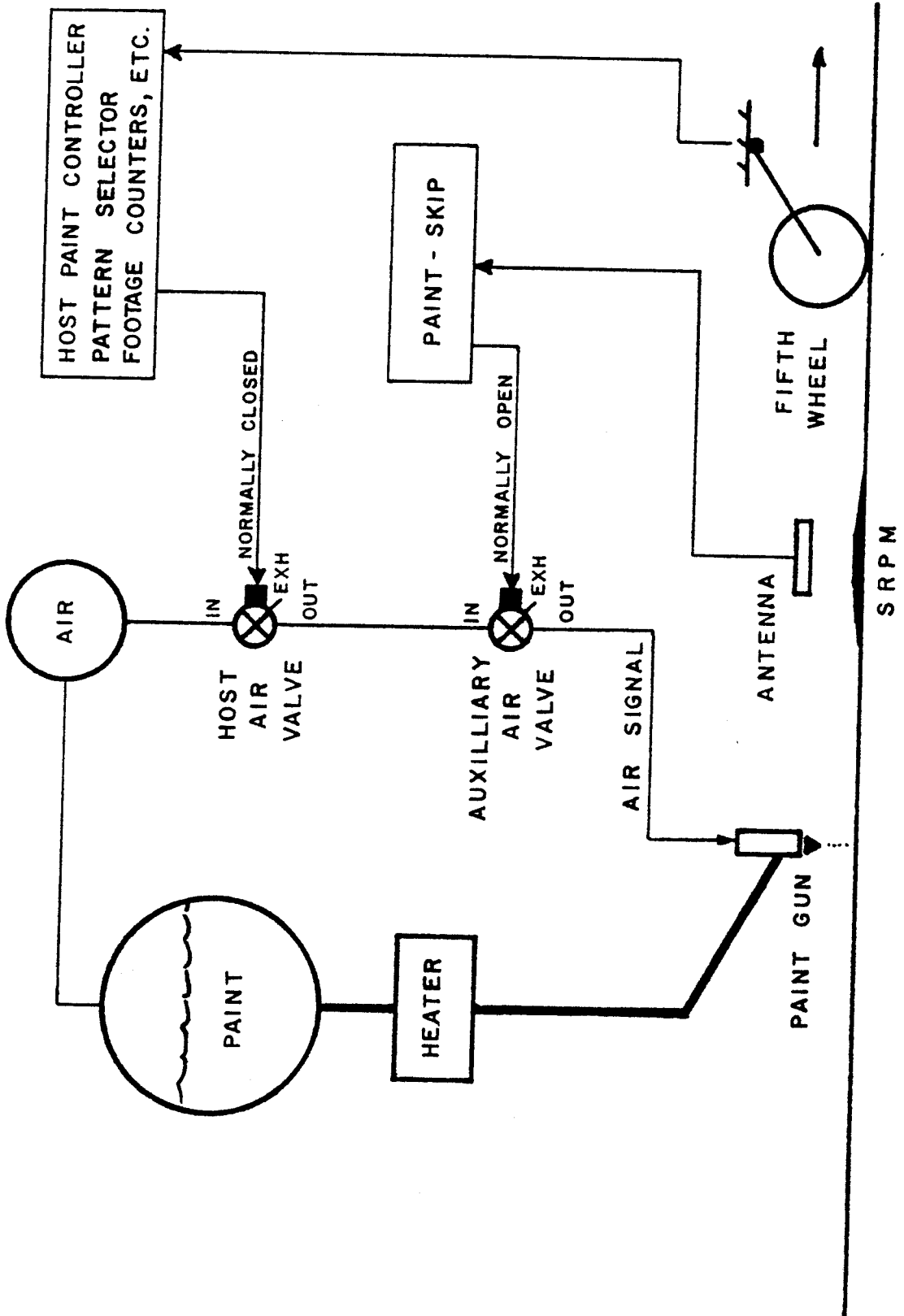


FIGURE 2

PAINT - SKIP

FUNCTIONAL BLOCK DIAGRAM

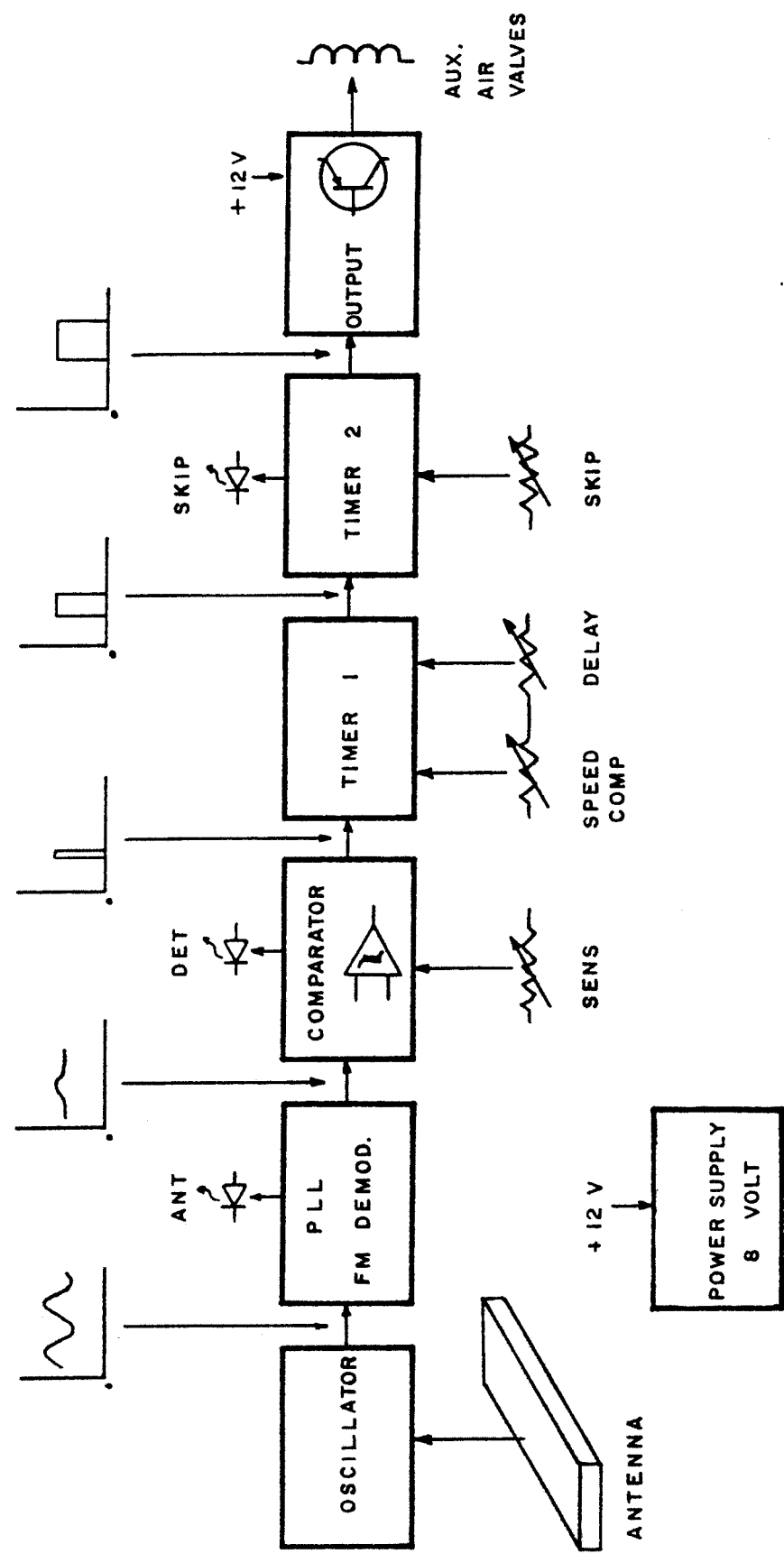
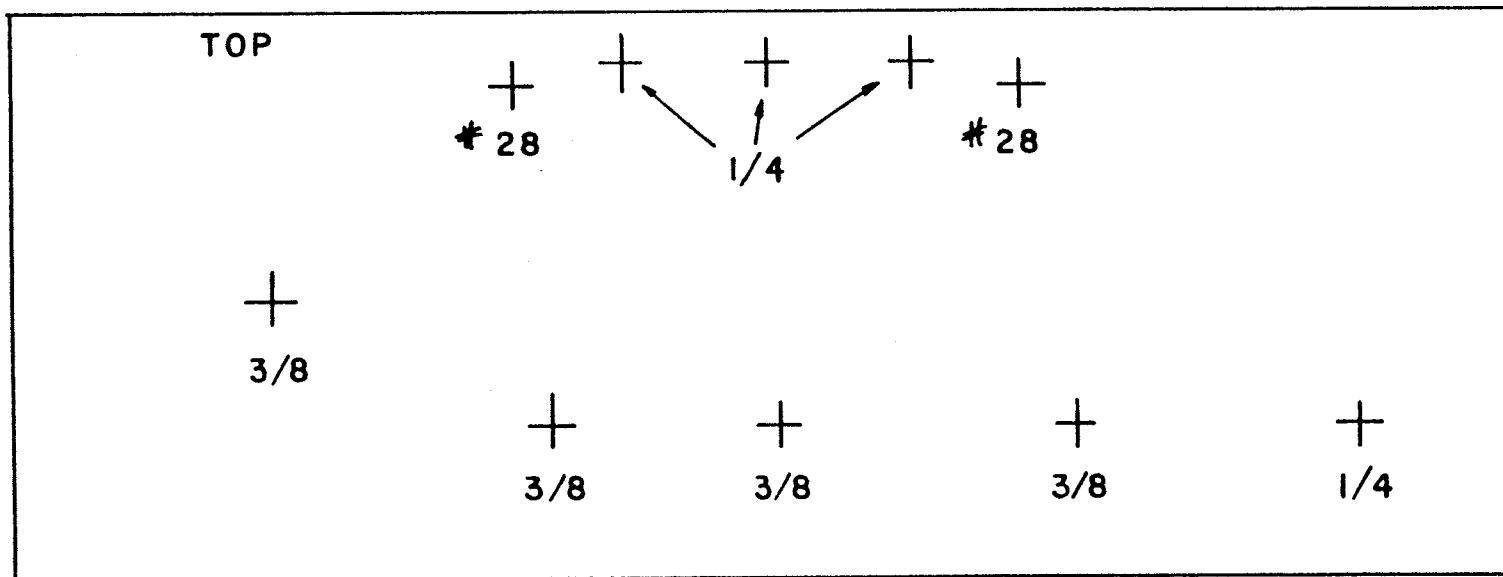


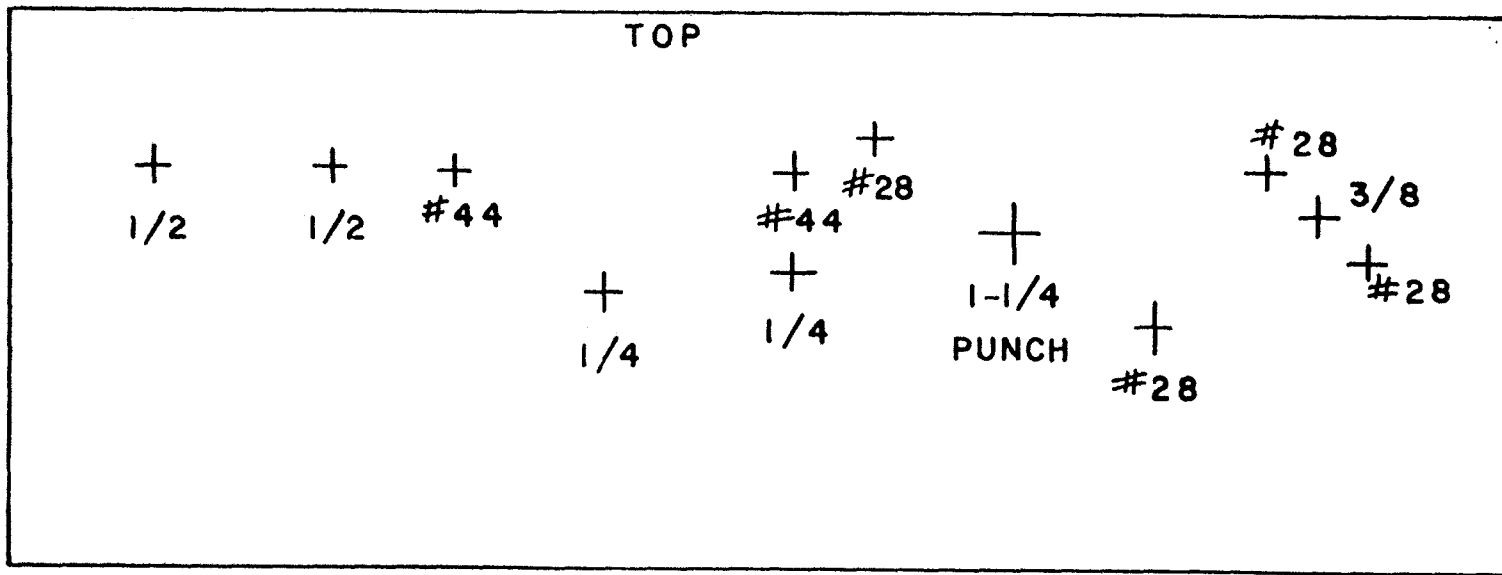
FIGURE 4
DRILL TEMPLATE - FRONT



FULL SIZE

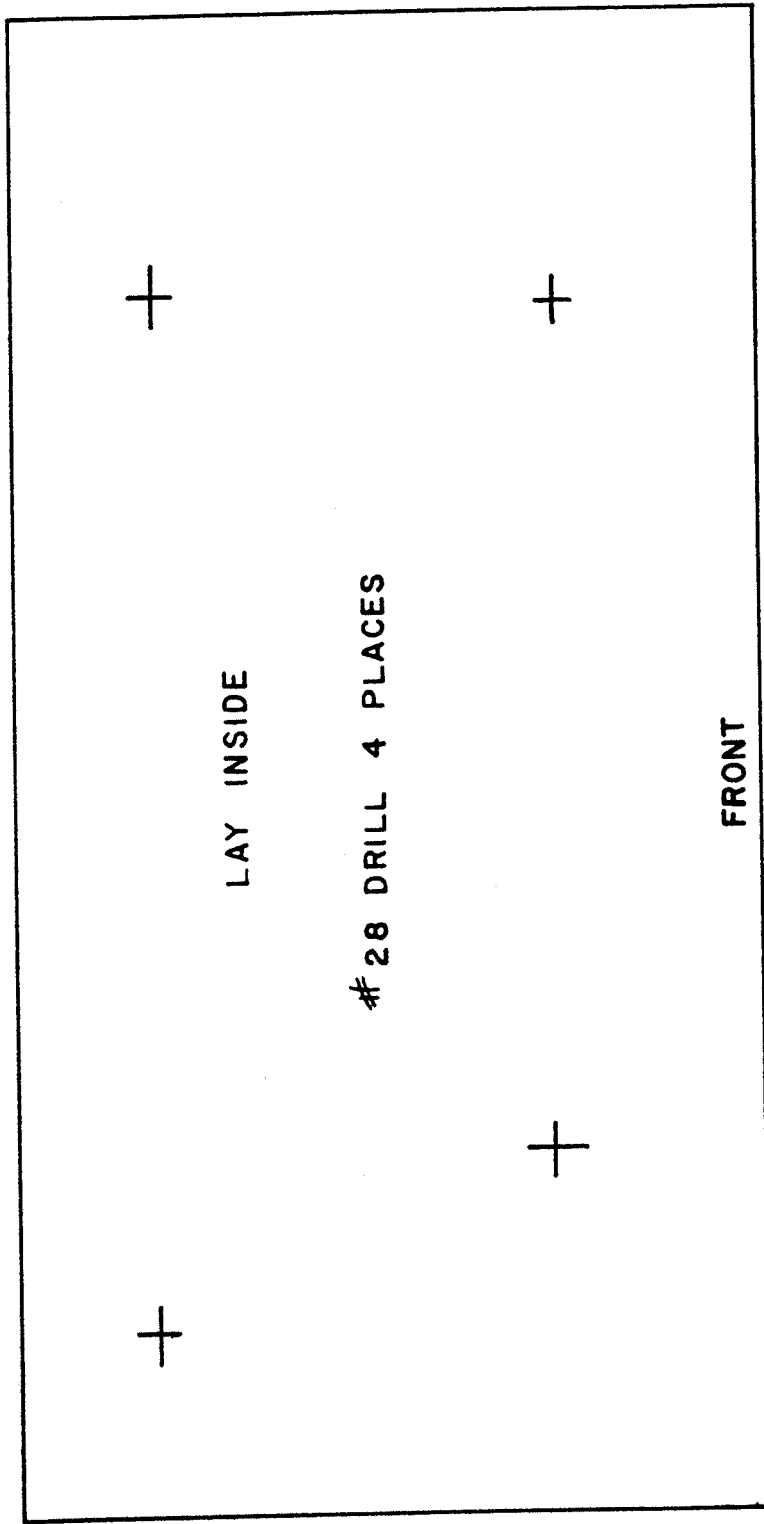
FIGURE 5

DRILL TEMPLATE - REAR



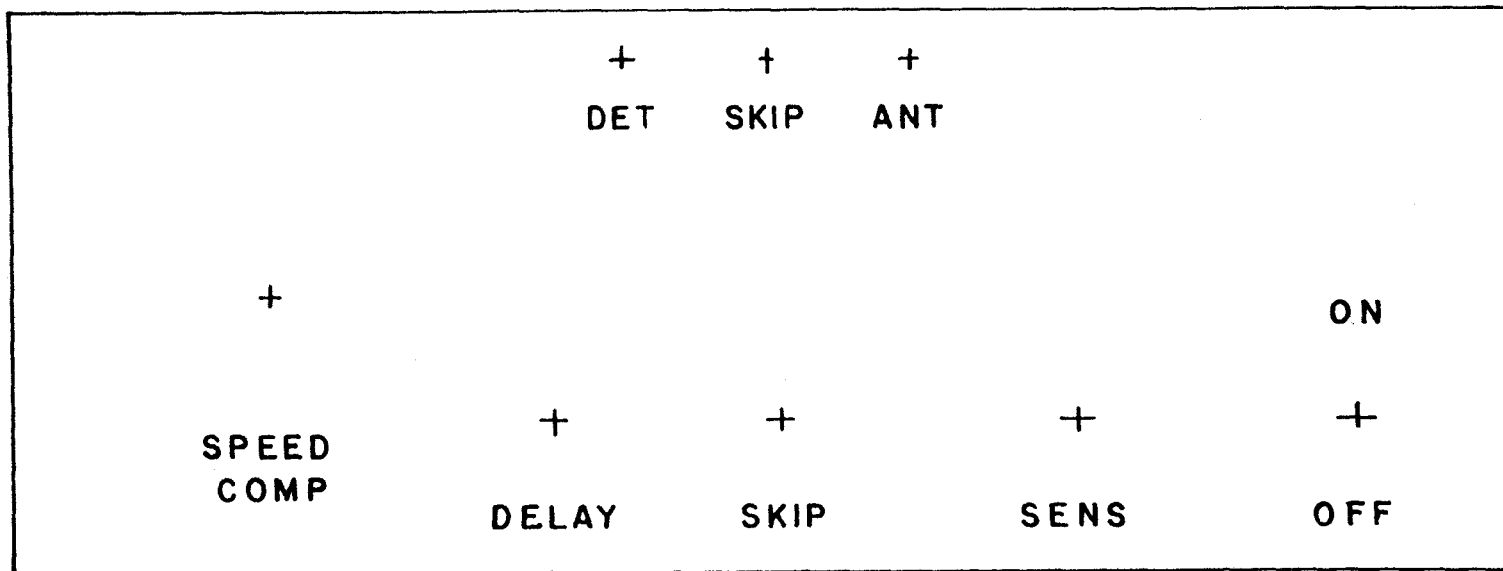
FULL SIZE

FIGURE 6
DRILL TEMPLATE - BOTTOM



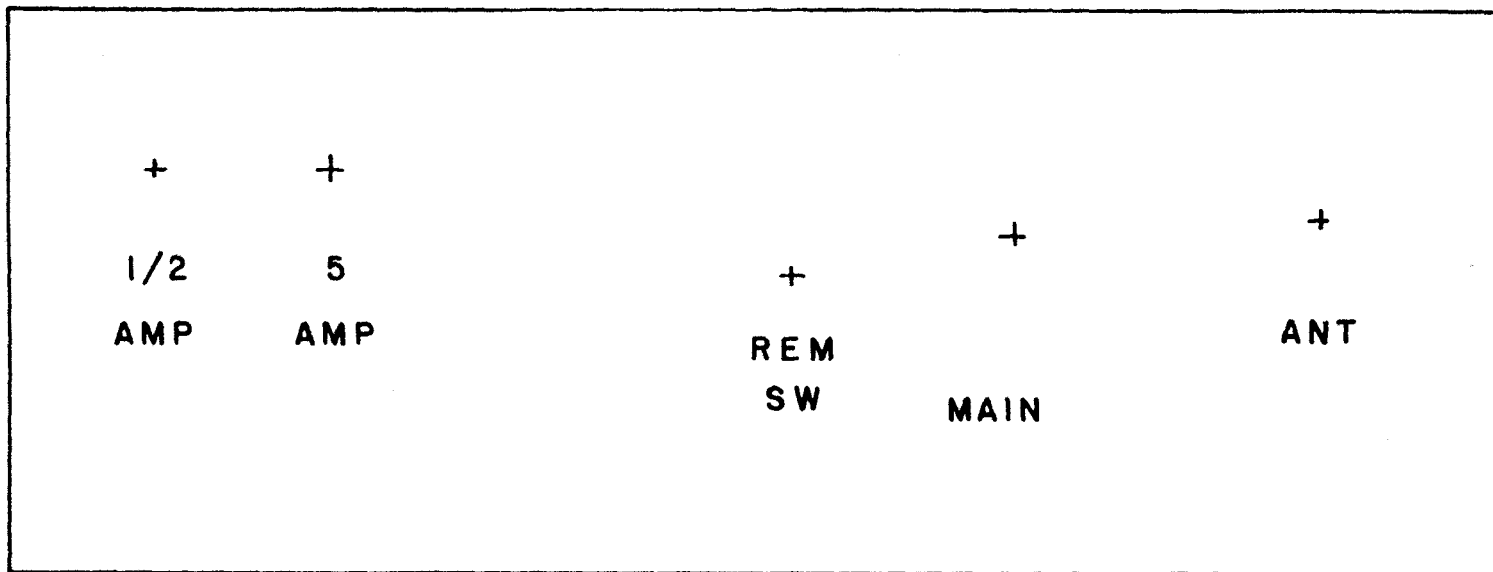
FULL SIZE

FIGURE 7
FRONT PANEL LETTERING



FULL SIZE

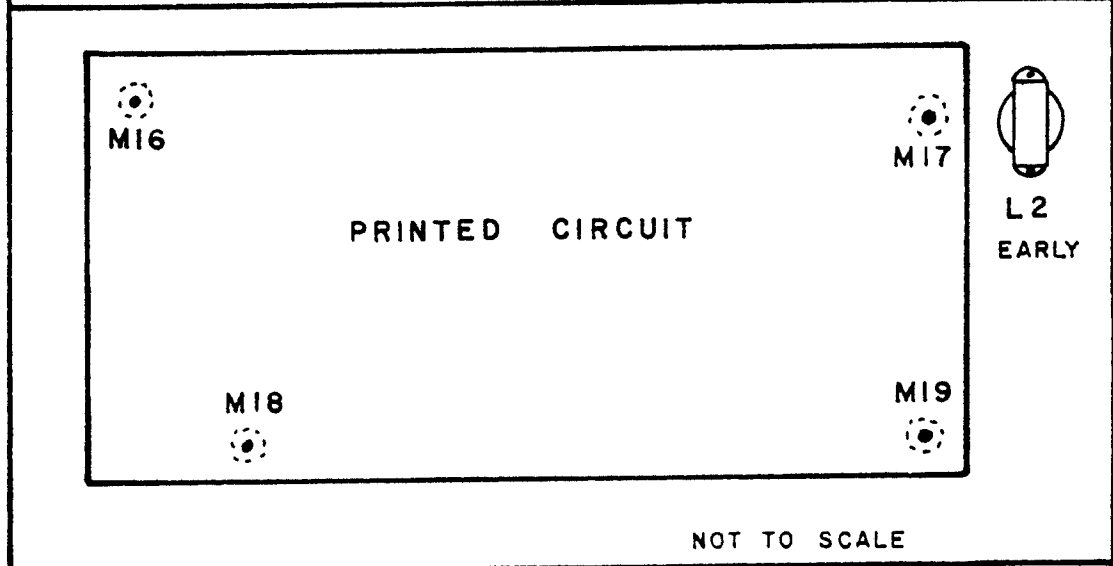
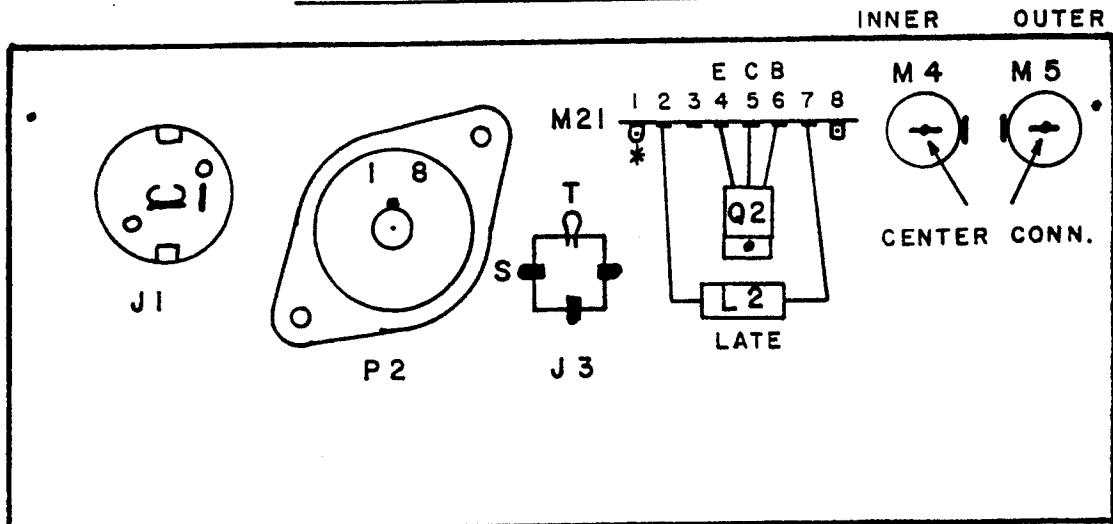
FIGURE 8
REAR PANEL LETTERING



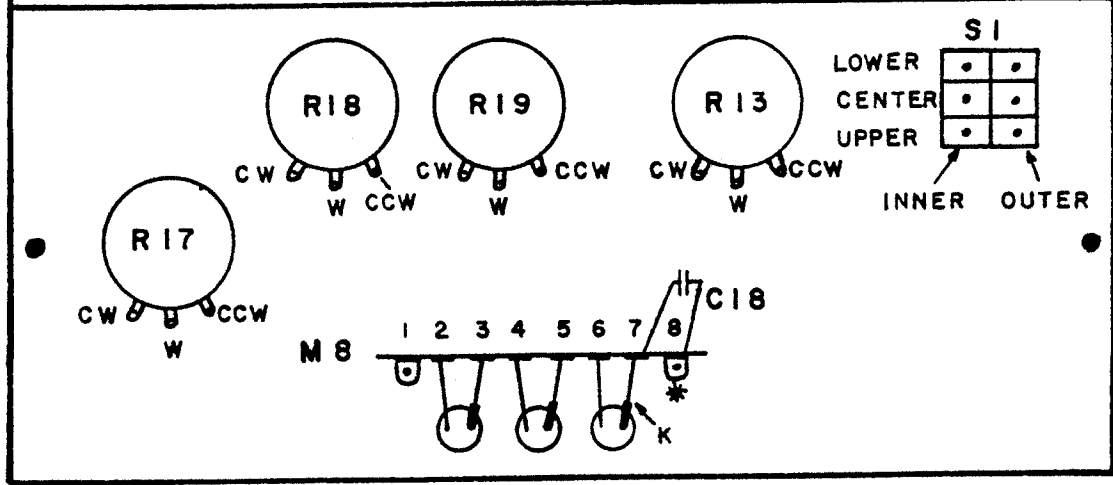
FULL SIZE

43

FIGURE 9
CHASSIS PARTS LAYOUT



NOT TO SCALE



M2 M3 M1 * USE LOCKWASHER LUG TO CHASSIS

VIEW WITH CHASSIS FLATTENED

FIGURE 10

PARTS PLACEMENT - COMPONENT SIDE

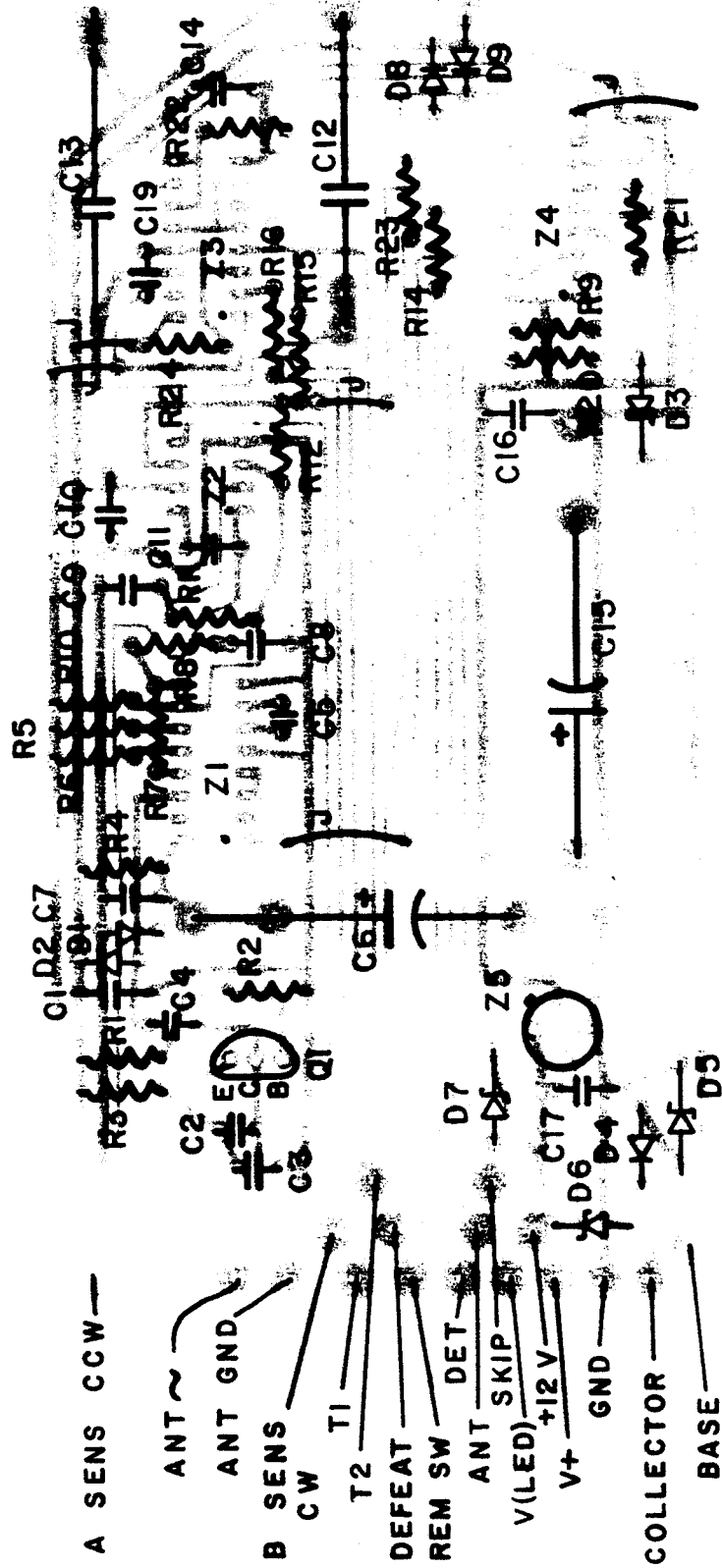


FIGURE 11

PARTS PLACEMENT - FOIL SIDE

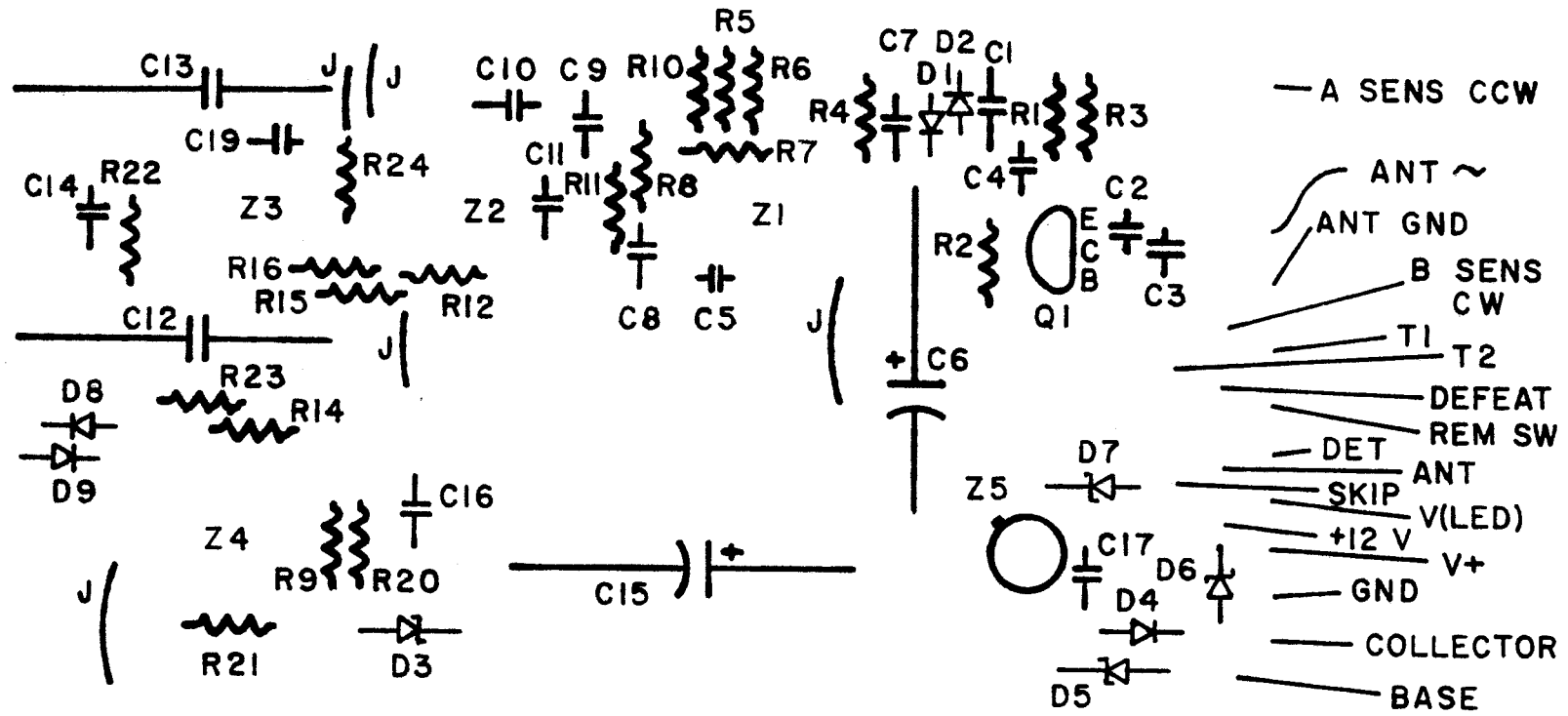
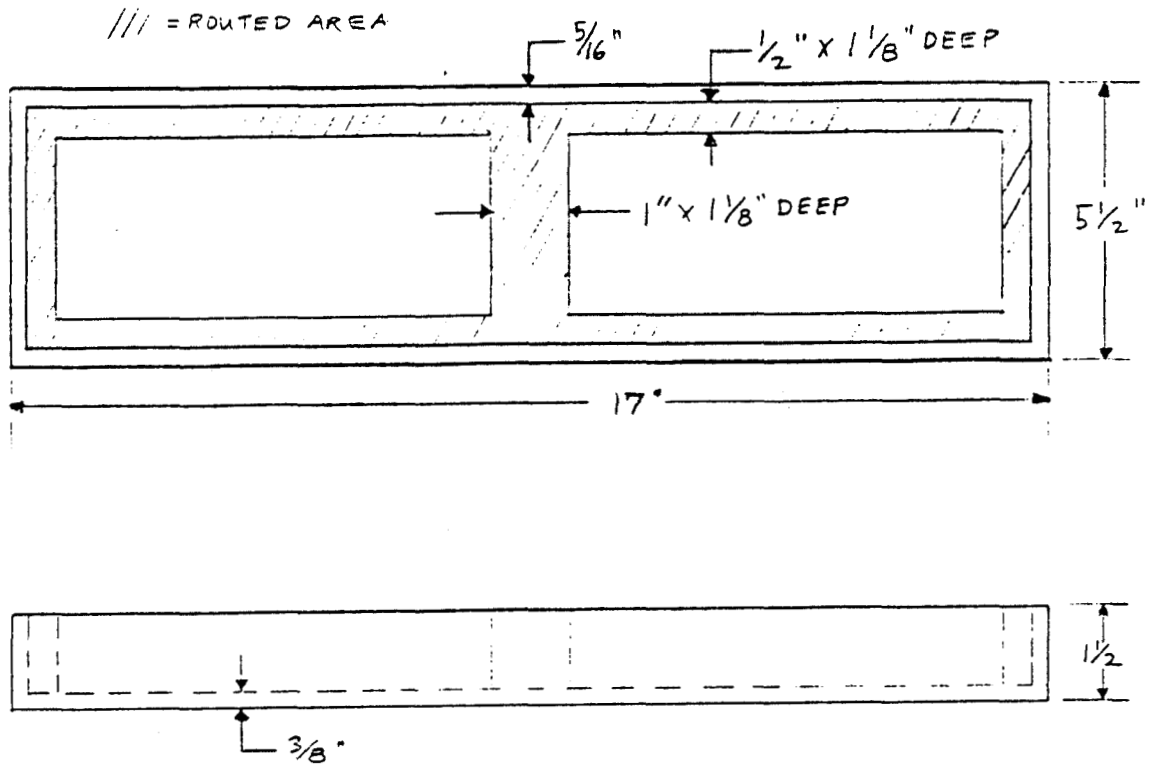


FIGURE 12
ANTENNA CONSTRUCTION



NOT TO SCALE

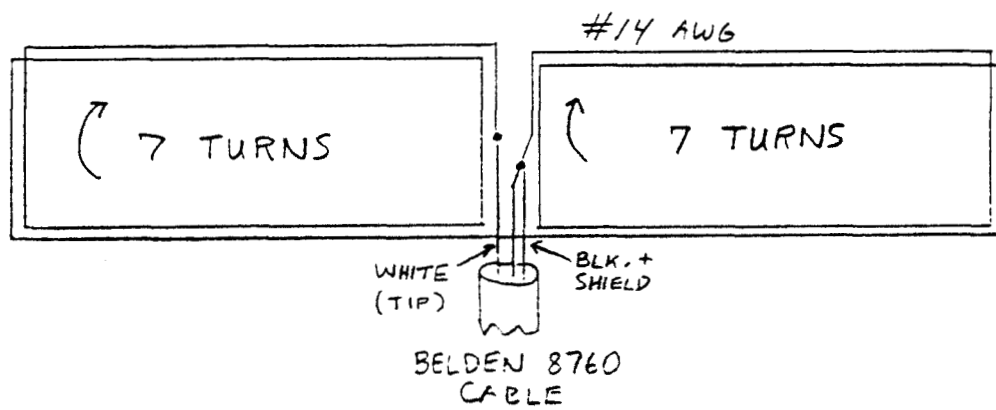


FIGURE 13
ASSEMBLY DRAWING

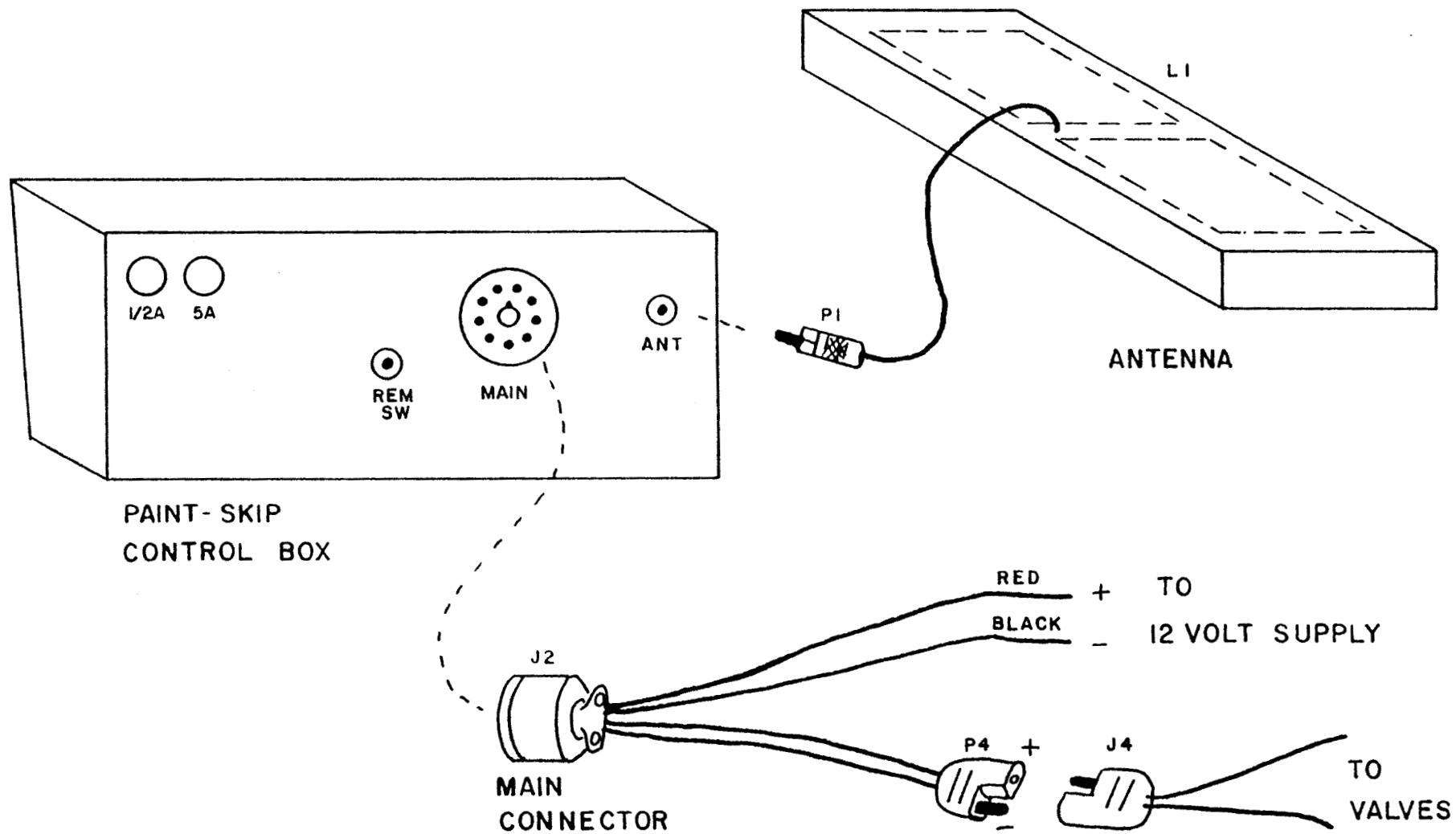
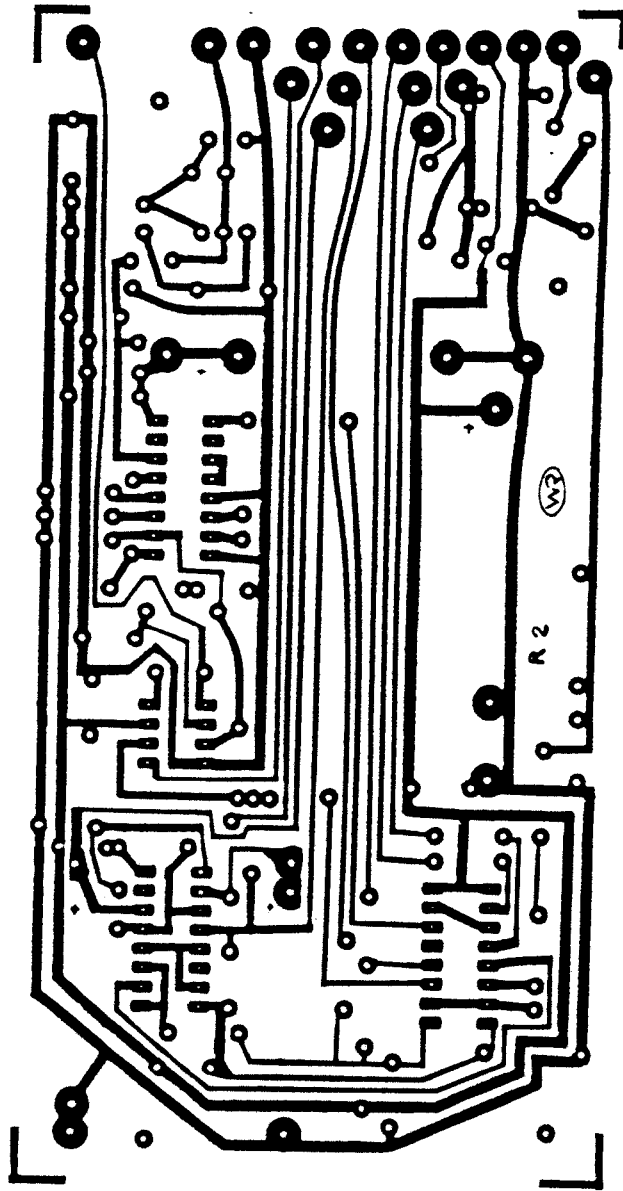


FIGURE 14

PRINTED CIRCUIT



APPENDIX B

PARTS LIST AND SOURCES OF SUPPLY

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Parts List and Recommended Spare Parts	51
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PARTS LIST

PART DESIGNATION	DESCRIPTION, MANUFACTURER, PART NO.
R1,2,5,16	RESISTOR, 10K OHM, CARBON COMPOSITION OR CARBON FILM, 1/4 WATT, 10% TOLERANCE OR BETTER, MFR. STACKPOLE, PANASONIC, OTHERS
R3	RESISTOR, 220 OHM, AS ABOVE
R4	RESISTOR, 180 OHM, AS ABOVE
R6	RESISTOR, 68K OHM, AS ABOVE
R7,10,15,22	RESISTOR, 100K OHM, AS ABOVE
R8	RESISTOR, 4.7K OHM, AS ABOVE
R9,14,20,21,23	RESISTOR, 1K OHM, AS ABOVE
R11,24(NOTE 1)	RESISTOR, 1M OHM, AS ABOVE
R12	RESISTOR, 220K OHM, AS ABOVE
R13	POTENTIOMETER, 100K OHM, LOCKING SHAFT CLARO 53C2-100K SUB OHMITE CLU-1041
R17	POTENTIOMETER, 250K OHM, PLAIN SHAFT CLARO 53C3-250K SUB CLARO 53C1-250K AND CUT SHAFT TO 1/2"
R 18,19	POTENTIOMETER, 1M OHM, LOCKING SHAFT CLARO 53C2-1M SUB OHMITE CLU-1052
** NOTE: 1K=1,000 1M=1,000,000 **	
** NOTE: SUB=SUBSTITUTE PERMITTED **	
C1,7,10,14,16	CAPACITOR, DISC CERAMIC, 0.01 MICROFARAD, 50 VOLT CRL UK50-103 SUB CRL CK-103
C2,3	CAPACITOR, MONOLITHIC, TEMPERATURE STABLE, 0.0047 MICROFARAD, 10% TOLERANCE, 50 VOLT CRL CW15C472K SUB CRL CW15A472K
C4,11	CAPACITOR, DISC CERAMIC, 50 PICOFARAD, 10% TOLERANCE, 1000 VOLT CRL DD-500 SUB CRL DD-510
C5	CAPACITOR, MONOLITHIC, TEMPERATURE STABLE, 100 PICOFARAD, 10% TOLERANCE, 50 VOLT CRL CN15A101K SUB MAL CK05BX101K
C6 (NOTE 2)	CAPACITOR, ELECTROLYTIC, 200 MICROFARAD, 16 VOLT SPRAGUE TVA-1160.6 SUB SPRAGUE TVA-1207.7

C8 CAPACITOR, MONOLITHIC, TEMPERATURE STABLE,
 0.01 MICROFARAD, 10% TOLERANCE, 50 VOLT
 CRL CW15C103K
 SUB MAL CK05BX103K

C9 (NOTE 3) CAPACITOR, MONOLITHIC, TEMPERATURE STABLE,
 0.018 MICROFARAD, 10% TOLERANCE, 50 VOLT
 MAL CK05BX183K
 SUB CRL CW20C183K

C12,13 CAPACITOR, METAL FILM,
 0.47 TO 0.5 MICROFARAD, 10% TOLERANCE, 50 VOLT
 CDE WMF05P47-10
 SUB CDE WMF05P5-10
 SUB CDE WMF1P47-10
 SUB CDE WMF1P50-10

C15 (NOTE 4) CAPACITOR, ELECTROLYTIC, 100 MICROFARAD, 16 VOLT
 SPRAGUE TVA-1160
 SUB SPRAGUE TVA-1207

C17,19 CAPACITOR, DIPPED TANTALUM, 1 MICROFARAD, 35 VOLT
 SPRAGUE 196D105X9035HA1
 SUB SPRAGUE 196D105X9050HA1
 SUB PANASONIC ECS-F35E1

C18 (NOTE 5) CAPACITOR, DISC CERAMIC,
 0.001 MICROFARAD, 10% TOLERANCE, 1000 VOLT
 CRL DD-102
 SUB SPRAGUE 5GA-D10

C20,21 (NOTE 6) CAPACITOR, DISC CERAMIC, 0.1 MICROFARAD, 50 VOLT
 CRL UK50-104
 SUB CRL CK-104

C22 (NOTE 6) CAPACITOR, DISC CERAMIC, 0.02 MICROFARAD, 50 VOLT
 CRL CK-203
 SUB CRL UK50-223

L1 ANTENNA COIL - SPECIAL CONSTRUCTION (SEE TEXT)

L2 (NOTE 7) HASH CHOKE, 500 MICROHENRIES, 0.26 OHM
 MILLER 5256
 SUB ANY SMALL E-CORE CHOKE, APPROX. 1 TO 4
 MILLIHENRIES, 1 AMPERE, TAB MOUNT

D1,2,8,9 RECTIFIER DIODE, 1N914 (GE, FAI)

D3,7 ZENER DIODE, 6.8 VOLT, 1 WATT, 1N4736A (MOT, TEL)

D4 RECTIFIER DIODE, 1N4007 (MOT)

D5,6 ZENER DIODE, 16 VOLT, 1 WATT, 1N4745A (MOT, TEL)

Q1 TRANSISTOR, PNP, 2N5355 (GE, MOT)

Q2 TRANSISTOR, PNP POWER DARLINGTON, TIP-126
 (MOT, TI)

Z1 INTEGRATED CIRCUIT, PHASE LOCK LOOP
 RCA CD4046BE
 SUB MOT MC14046BCP

Z2 INTEGRATED CIRCUIT, OPERATIONAL AMPLIFIER
RCA CA3130AE
SUB RCA CA3130AS

Z3 INTEGRATED CIRCUIT, DUAL TIMER
RCA CD4538BE
SUB MOT MC14538BCP

Z4 INTEGRATED CIRCUIT, HEX INVERTING BUFFER
RCA CD4049BE OR -UBE
SUB MOT MC14049BCP

Z5 INTEGRATED CIRCUIT, VOLTAGE REGULATOR, 8 VOLT
MOT MC78L08CG
SUB MOT MC78L08ACG
SUB MOT MC78L08CP, -ACP (DIFFERENT LEAD PATTERN)

S1 SWITCH, MINIATURE TOGGLE, SEALED HANDLE, DPDT
ALCO MTE-206N

P1 PLUG, "RCA PHONO", SWC 3502

J1 JACK, "RCA PHONO", SWC 3501F

P2 (NOTE 8) PLUG, OCTAL, AMPHENOL 86-CP8

J2 (NOTE 8) JACK ASSEMBLY, OCTAL, WITH FLANGE AND RETAINER
AMPHENOL 78RS8

J3 JACK, MINIATURE 1/8 INCH, ENCLOSED, SWC 142A
SUB SWC 41

P4, J4 TWO CONDUCTOR POLARIZED CONNECTOR SET
COLE-HERSEE 11172 (AUTOMOTIVE PARTS STORES)

M1,2,3 LIGHT EMITTING DIODE, GENERAL INSTRUMENTS CMD-5022

M4,5 FUSE HOLDER, BUSS HKP

M6 ENCLOSURE, BUD SC-3032

M7 SOLDER, ERSIN "MULTICORE" OR OTHER HIGH QUALITY
"RADIO" SOLDER

M8 TERMINAL STRIP, TRW 56A

M9 SOCKET, 8-PIN DUAL INLINE
AUGAT 208AG29D
SUB MAL DILB8P11

M10a,b,c SOCKET, 16-PIN DUAL INLINE
AUGAT 216AG29D
SUB MAL DILB16P11

M11 FUSE, BUSS AGC 1/2

M12 FUSE, BUSS AGC 5

M13 HOOKUP WIRE, 22 AWG STRANDED, BELDEN 8524

M14 KNOB, KURZ-KASCH S-292-1L

M15 SCREW, NYLON, #6-32 X 5/8", ROUND HEAD
SMITH 2524
SUB CONCORD 701-6626

M16-19 STANDOFF, ALUMINUM, 1/4" HEX, INTERNAL THREAD
#6-32, 5/8" LONG, SMITH 8424
SUB CONCORD 635A-7610-19

M20 CAP FOR J2, AMPHENOL 86-3-24

M21 TERMINAL STRIP, MINIATURE, SMITH 1075
SUB CONCORD 707-5129

M22	"SPAGHETTI" WIRE INSULATION, 1/16" I.D.	
M23	FASTENERS, STEEL, PLATED	
	a. SCREW, PAN HEAD, #6-32 X 1/4"	14 REQ.
	b. LOCKWASHER, INTERNAL TOOTH, #6	11 REQ.
	c. NUT, HEX, #6-32	6 REQ.
	d. SCREW, ROUND HEAD, #2-56 X 1/4"	2 REQ.
	e. LOCKWASHER, INTERNAL TOOTH, #2	3 REQ.
	f. NUT, HEX, #2-56	2 REQ.
	g. FLAT WASHER, 3/8" I.D. X 1 1/16" O.D.	4 REQ.
M24	MOUNTING HARDWARE FOR Q2 (MICA INSULATOR, STEP WASHER, SPACER), RCA KC31B	
M25	WIRE, MAGNET, FOR L2, BELDEN 8073 (1 LB. ROLL MAKES THREE ANTENNAS)	
M26	PAINT, FOR ENCLOSURE TOP, ANY SPRAY ENAMEL SUCH AS RUST OLEUM 7745 SUNSET YELLOW	
M27	PRINTED CIRCUIT BOARD (SPECIAL-SEE FIGURE 14)	
M28	TRANSFER LETTERS, DATAK 9601	
M29	SPRAY FINISH FOR M28, DATAK 04177	
M30a, b, c	MOUNTING HARDWARE FOR M1, 2, 3	
	GENERAL INSTRUMENTS CMP-22	
M31	WIRE, 2 CONDUCTOR SHIELDED, FOR L1 BELDEN 8760 (ABOUT 17' PER ANTENNA)	
M32	SHRINK TUBE, 1/2" X 1 7/16" LONG, ALPHA FIT 221-1/2"	
M33	SHRINK TUBE, 1/8", ALPHA FIT 221-1/8"	
M34	WOOD FOR MAKING ANTENNA L1, STANDARD 2X6" PLANK, CLEAR, STRAIGHT, 17" LONG	
M35	POTTING MATERIAL FOR L1 ANTENNA, USE ANY RIGID-SETTING EPOXY SUCH AS THAT USED TO INSTALL SRPMs	
M36	WIRE, RED, AUTOMOTIVE PRIMARY, 16 AWG (J2 REQUIRES 19")	
M37	WIRE, BLACK, AUTOMOTIVE PRIMARY, 16 AWG (J2 REQUIRES 19")	
M38	HEAT SINK COMPOUND, GENERAL CEMENT DC-Z9	
M39	AUXILLIARY AIR VALVE, 12 VOLTS DC, NORMALLY-OPEN, THREE-WAY, FLANGE MOUNT, 1/4" ORIFICE, HUMPHREY 250E1-3-11-21-35-61 (12VDC)	
M40	MUFFLER FOR PROTECTION OF M39 EXHAUST PORT FROM DIRT ENTRY, SINTERED BRONZE, HUMPHREY EM2	
M41	1/4" ID HOSES, NIPPLES, CLAMPS AND OTHER FITTINGS AND FASTENERS FOR INSTALLATION OF M39	

NOTES:

1. PRIOR TO SERIAL #107 R24 WAS 100K OHM
2. PRIOR TO SERIAL #107 C6 WAS 640 MICROFARAD
3. PRIOR TO SERIAL #107 C9 WAS 0.2 MICROFARAD DISC CERAMIC.
THE CHANGE WAS MADE NECESSARY BY PART MANUFACTURER'S
CHANGE IN SPECIFICATION FOR THE PART.
4. PRIOR TO SERIAL #107 C15 WAS 1000 MICROFARAD
5. PRIOR TO SERIAL #107 C18 WAS 220 PICOFARAD.
THE CHANGE WAS MADE TO SUPPRESS A SLIGHT GLOW IN LED M1
UNDER NORMAL CONDITIONS FOR SOME UNITS.
6. C20,21 AND 22 WERE ADDED AFTER SERIAL #106 TO IMPROVE NOISE
IMMUNITY.
7. PRIOR TO SERIAL #107, L2 WAS A SMALL E-CORE UNIT AS DESCRIBED.
CHANGE OF CHOKE L2 AND REVISED MOUNTING OF L2 WERE MADE
NECESSARY BY PART MANUFACTURER'S DROPPING THE PART.
8. P2 AND J2 ARE TO BE MODIFIED AS DESCRIBED IN THE TEXT.

R24, C6 AND C15 NEED NOT BE CHANGED UNLESS A PROBLEM ARISES
WITH UNDESIRE SKIPS AT TURN-ON. IN THAT CASE, UPGRADE ALL THREE
PARTS.

LIST OF RECOMMENDED SPARE PARTS

ONE EACH: P1, J1, Q1, Q2, Z1-Z5, D6, R13, R17, R18/19, L1 ASSEMBLY,
S1, M11, M12

SOURCES OF SUPPLY

This list will identify the manufacturers given in the parts list, some of which were given abbreviated names to save space.

Source: 1984/85 editions
of Gold Book and EEM.

1. ELECTRONIC DESIGN'S "GOLD BOOK"
HAYDEN PUBLISHING COMPANY
50 ESSEX STREET
ROCHELLE PARK, NJ 07662
201-843-0550
2. EEM, ELECTRONIC ENGINEERS MASTER
HEARST BUSINESS COMMUNICATIONS, INC./UTP DIVISION
645 STEWART AVE.
GARDEN CITY, NY 11530
516-222-2500

ALCO ELECTRONIC PRODUCTS, INC.
1551 OSGOOD ST.
N. ANDOVER, MA 01845 617-685-4371

ALPHA WIRE CORP.
711 LIDGERWOOD AVE. P.O. BOX 711
ELIZABETH, NJ 07207 201-925-8000

AMPHENOL, AN ALLIED CO.
2122 YORK RD.
OAK BROOK, IL 60521 312-986-1200

AUGAT, INC.
33 PERRY AVE., BOX 779
ATTLEBORO, MA 02703 617-222-2202

BELDEN ELECTRONIC WIRE AND CABLE
P.O. BOX 1980
RICHMOND, IN 47375 317-983-5200

BUD RADIO
4605 E. 355th ST.
WILLOUGHBY, OH 44094 216-946-3200

BUSSMAN DIV. (BUSS)
P.O. 14460
ST. LOUIS, MO 63178 314-394-2877

CENTRALAB, INC. (CRL)
5855 NORTH GLEN PARK ROAD
MILWAUKEE, WI 53209 414-228-7380

CLAROSTAT MFG. (CLARO)
WASHINGTON ST.
DOVER, NH 03820 603-742-1120

COLE-HERSEE CO. (AVAILABLE IN AUTO PARTS STORES)
20 OLD COLONY AVE.
BOSTON, MA 02127 617-268-2100

CONCORD ELECTRONICS
30 GREAT JONES ST.
NEW YORK, NY 10012 212-777-6571

DATAK CORP.
65 71st ST.
GUTTENBURG, NJ 07093 201-869-2200

FAIRCHILD CAMERA AND INSTRUMENT CORP. (FAI)
464 ELLIS ST., MS15-1035
MOUNTAIN VIEW, CA 94042 415-962-5011

GENERAL CEMENT
400 SOUTH WYMAN ST.
ROCKFORD, IL 61101 815-968-9661

GENERAL ELECTRIC (GE)
W. GENESSEE ST.
AUBURN, NY 13021 315-253-7321

GENERAL INSTRUMENTS
600 W. JOHN ST.
HICKSVILLE, NY 11802 516-733-3107

HUMPHREY PRODUCTS
KILGORE AT SPRINKLE P.O. BOX 2008
KALAMAZOO, MI 49003 616-381-5500

KURZ-KASCH
711 HUNTER DR.
WILMINGTON, OH 45177 513-382-0966

MALLORY CAPACITOR CO. (MAL)
3029 E. WASHINGTON ST.
INDIANAPOLIS, IN 46201 317-636-5353

J.W. MILLER DIV., BELL INDUSTRIES
19070 REYES AVE. P.O. BOX 5825
RANCHO DOMINGUEZ, CA 90224 213-537-5200

MOTOROLA SEMICONDUCTOR PRODUCTS (MOT)
 BOX 20912
 PHOENIX, AZ 85036 602-244-6900

OHMITE MFG. CO.
 3601 HOWARD ST.
 SKOKIE, IL 60076 312-675-2600

PANASONIC IND'L. ELECTRONIC COMPONENTS
 BOX 1503
 SECAUCUS, NJ 07094 201-348-7000

RCA SOLID STATE DIV.
 ROUTE 202
 SOMERVILLE, NJ 08876 201-685-6000

H.H. SMITH (KULKA-SMITH, INC.) (SMITH)
 1913 ATLANTIC AVE.
 MANASQUAN, NJ 08736 201-223-9400

SPRAGUE ELECTRIC CO.
 481 MARSHALL ST.
 NO.ADAMS, MA 01247 413-664-4411

STACKPOLE CORP.
 STACKPOLE ST.
 ST. MARYS, PA 15857 814-781-1234

SWITCHCRAFT, INC. (SWC)
 5555 N. ELSTON
 CHICAGO, IL 60630 312-792-2700

TELEDYNE SEMICONDUCTOR (TEL)
 1300 TERRA BELLA AVE.
 MOUNTAIN VIEW, CA 94040 415-968-9241

TEXAS INSTRUMENTS, INC. (TI)
 BOX 225012-MS-84
 DALLAS, TX 75265 214-995-6611

TRW CONNECTOR DIV.
 1501 MORSE AVE.
 ELK GROVE VILLAGE, IL 60007 312-981-6000

APPENDIX C

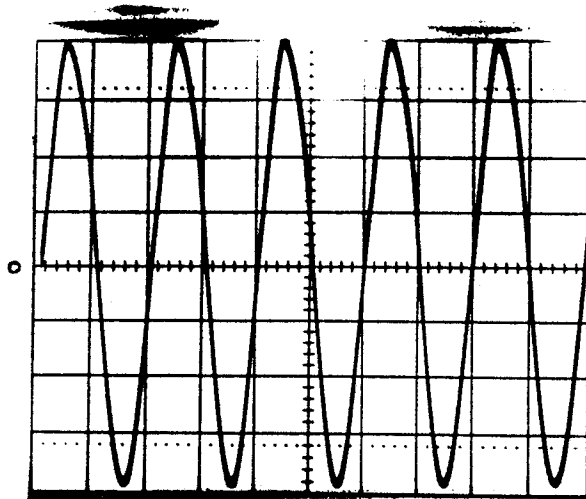
WAVEFORM PICTORIALS

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Waveform 1	60
Waveform 2	60
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Waveform 4	61
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Waveform 6	62
Waveform 7	63
Waveform 8	63
Waveform 9	64
Waveform 10	64

THE FOLLOWING PHOTOGRAPHS WERE MADE OF ACTUAL OSCILLOSCOPE TRACES FROM A WORKING PAINT-SKIP. PROBE CONNECTIONS AND OSCILLOSCOPE SETTINGS ARE LISTED FOR EACH WAVEFORM. UNLESS OTHERWISE NOTED,

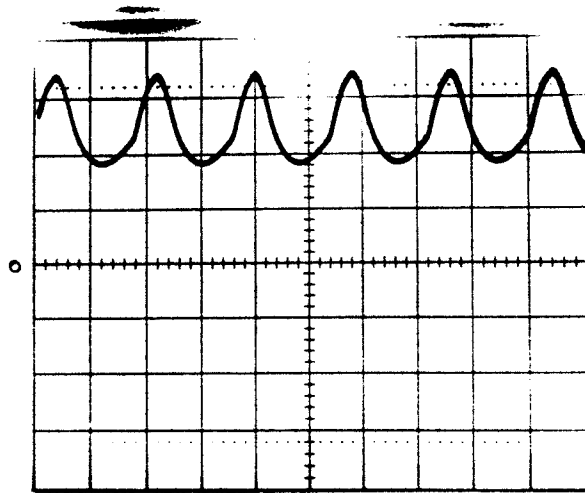
1. CHANNEL B IS THE LOWER TRACE, AND IS USED FOR THE TRIGGER SIGNAL, + SLOPE.
2. WAVEFORMS ARE TAKEN WITH RESPECT TO CHASSIS GROUND, DC COUPLED VERTICAL AMPLIFIERS.
3. INPUT IMPEDANCE IS 1 MEGOHM IN PARALLEL WITH 20 PICO FARADS.
4. PAINT-SKIP CONTROL SETTINGS:

SPEED COMP	50%
DELAY	0%
SKIP	50%



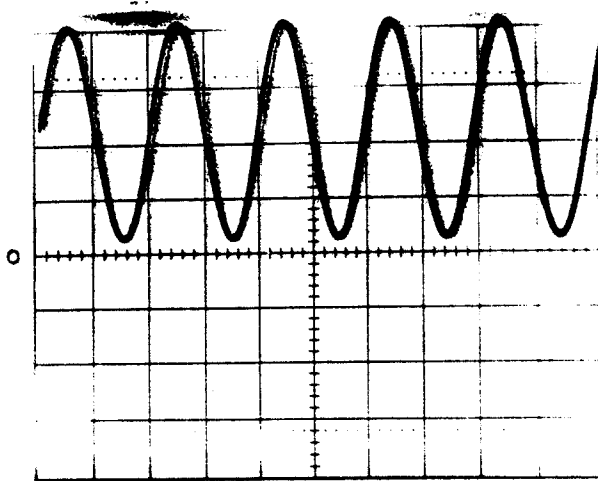
WAVEFORM 1

HORIZONTAL: 1 MICROSECOND/DIVISION
CHANNEL A: 2 VOLTS/DIVISION AT Q1 (COLLECTOR)



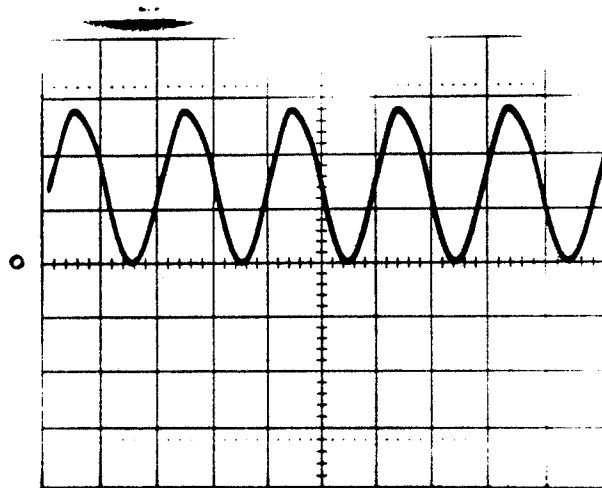
WAVEFORM 2

HORIZONTAL: 1 MICROSECOND/DIVISION
CHANNEL A: 2 VOLTS/DIVISION AT Q1 (BASE)



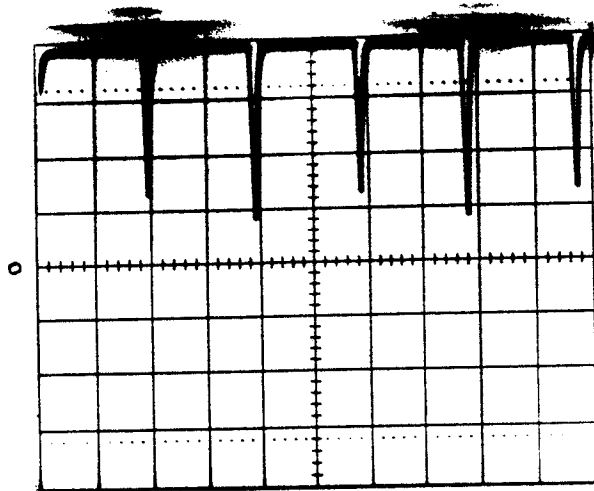
WAVEFORM 3

HORIZONTAL: 1 MICROSECOND/DIVISION
CHANNEL A: 2 VOLTS/DIVISION AT Q1 (EMITTER)



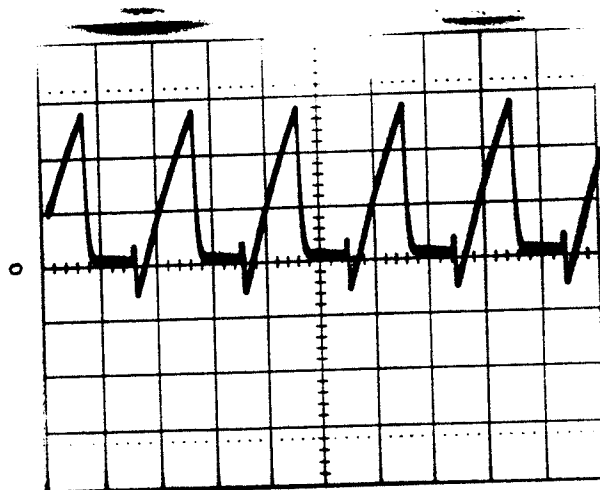
WAVEFORM 4

HORIZONTAL: 1 MICROSECOND/DIVISION
CHANNEL A: 2 VOLTS/DIVISION AT Z1 (PIN 14)



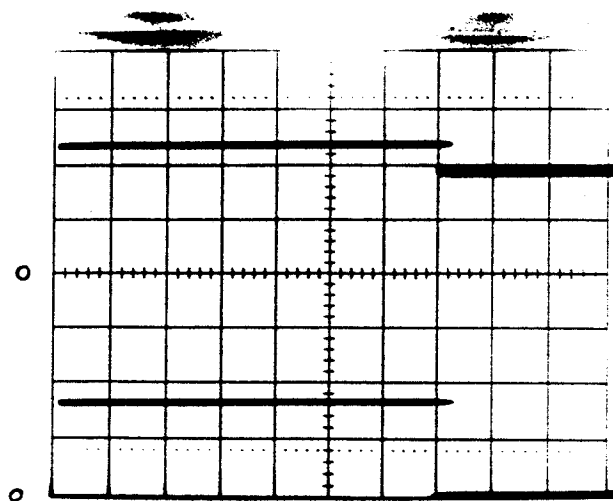
WAVEFORM 5

HORIZONTAL: 1 MICROSECOND/DIVISION
CHANNEL A: 2 VOLTS/DIVISION AT Z1 (PIN 1)



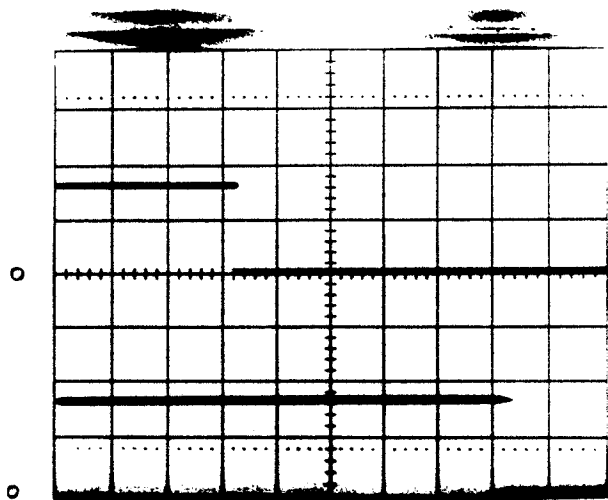
WAVEFORM 6

HORIZONTAL: 1 MICROSECOND/DIVISION
CHANNEL A: 2 VOLTS/DIVISION AT Z1 (PIN 6 OR 7)



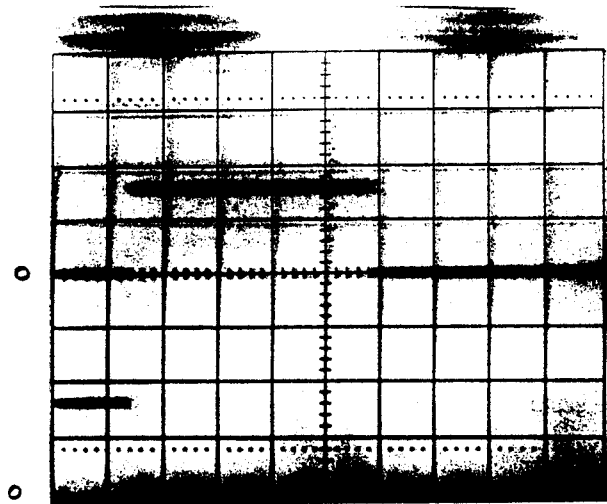
WAVEFORM 7

HORIZONTAL: 20 MILLISECONDS/DIVISION
CHANNEL A: 1 VOLT/DIVISION AT Z1 (PIN 10)
CHANNEL B: 5 VOLTS/DIVISION AT Z2 (PIN 6)



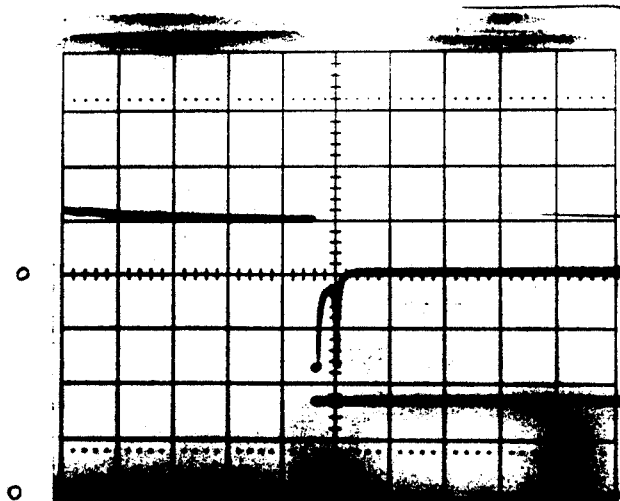
WAVEFORM 8

HORIZONTAL: 20 MILLISECONDS/DIVISION
CHANNEL A: 5 VOLTS/DIVISION AT Z3 (PIN 6)
CHANNEL B: 5 VOLTS/DIVISION AT Z2 (PIN 6)



WAVEFORM 9

HORIZONTAL: 50 MILLISECONDS/DIVISION
 CHANNEL A: 5 VOLTS/DIVISION AT Z3 (PIN 10)
 CHANNEL B: 5 VOLTS/DIVISION AT Z3 (PIN 6)



WAVEFORM 10

HORIZONTAL: 50 MILLISECONDS/DIVISION
 CHANNEL A: 10 VOLTS/DIVISION AT Q2 (COLLECTOR)
 CHANNEL B: 5 VOLTS/DIVISION AT Z3 (PIN 9)
 TRIGGER IS CHANNEL B, - SLOPE

APPENDIX D

SEMICONDUCTOR CATALOG PAGES

	PAGE
Q2-Transistor, PNP Power Darlington	66
Z1-Integrated Circuit, Phase Lock Loop	71
Z2-Integrated Circuit, Operational Amplifier	76
Z3-Integrated Circuit, Dual Timer	81
Z4-Integrated Circuit, Hex Inverting Buffer	90
Z5-Integrated Circuit, Voltage Regulator	94

NPN PNP
TIP120 TIP125
TIP121 TIP126
TIP122 TIP127

REPRODUCED COURTESY OF MOTOROLA, INC.

**PLASTIC MEDIUM-POWER
 COMPLEMENTARY SILICON TRANSISTORS**

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
 $V_{CE(sus)} = 60$ Vdc (Min) – TIP120, TIP125
 $= 80$ Vdc (Min) – TIP121, TIP126
 $= 100$ Vdc (Min) – TIP122, TIP127
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc
 $= 4.0$ Vdc (Max) @ $I_C = 5.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

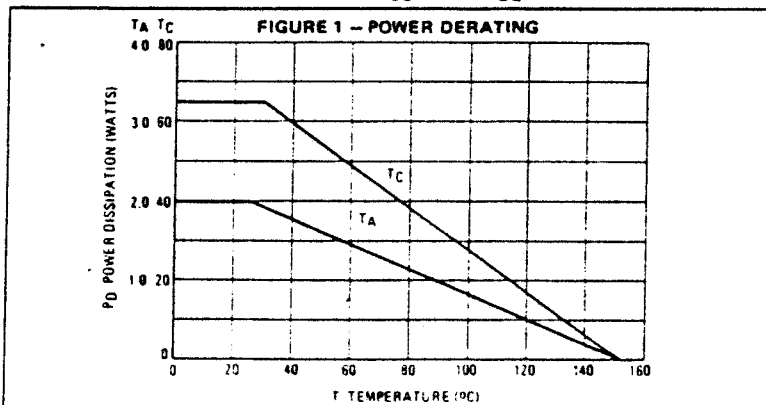
***MAXIMUM RATINGS**

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	5.0			Adc
Peak		8.0			
Base Current	I_B	120			mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	65			Watts
Derate above 25°C		0.52			W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0			Watts
Derate above 25°C		0.016			W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

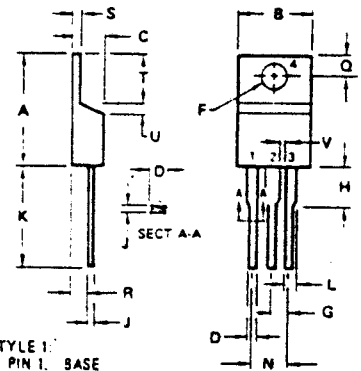
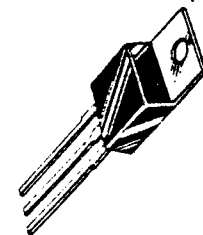
Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

(1) $I_C = 1$ A, $L = 100$ mH, P.R.F. = 10 Hz, $V_{CC} = 20$ V, $R_{BE} = 100 \Omega$.



**DARLINGTON
 8 AMPERE
 COMPLEMENTARY SILICON
 POWER TRANSISTORS**

60-80-100 VOLTS
 65 WATTS



STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

CASE Z21A-02
 TO-220AB

TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	60 80 100	— — —	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0)	I _{CEO}	— — —	0.5 0.5 0.5	mA
Collector Cutoff Current (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	I _{CBO}	— — —	0.2 0.2 0.2	mA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	2.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 0.5 A, V _{CE} = 3.0 Vdc) (I _C = 3.0 A, V _{CE} = 3.0 Vdc)	h _{FE}	1000 1000	— —	—
Collector-Emitter Saturation Voltage (I _C = 3.0 A, I _B = 12 mA) (I _C = 5.0 A, I _B = 20 mA)	V _{CE(sat)}	— —	2.0 4.0	Vdc
Base-Emitter On Voltage (I _C = 3.0 A, V _{CE} = 3.0 Vdc)	V _{BE(on)}	—	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I _C = 3.0 A, V _{CE} = 4.0 Vdc, f = 1.0 MHz)	h _{fe}	4.0	—	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2%.

FIGURE 2 - SWITCHING TIMES TEST CIRCUIT

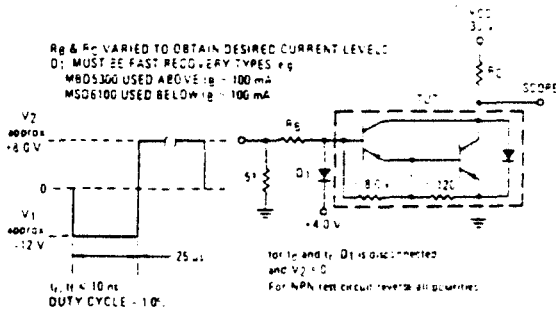
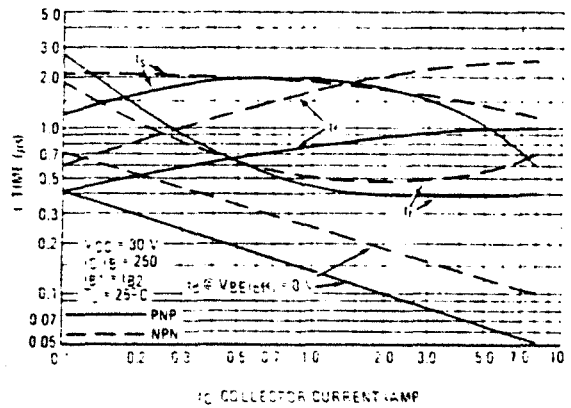


FIGURE 3 - SWITCHING TIMES



TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP

FIGURE 4 - THERMAL RESPONSE

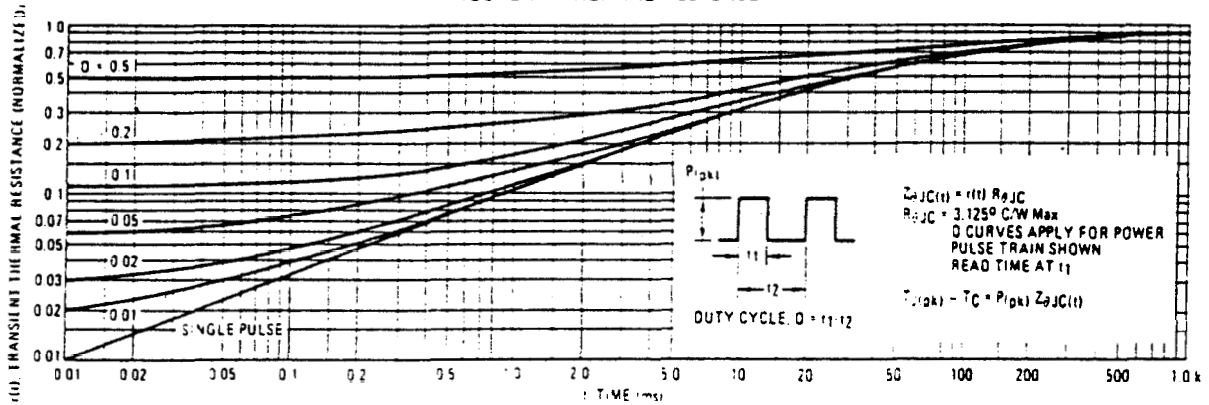
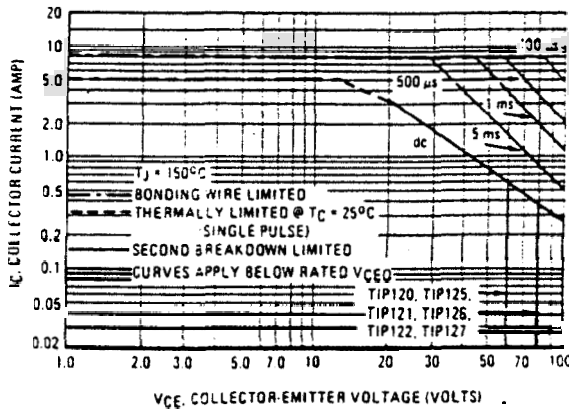


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{j(pk)} = 150^\circ C$; T_c is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} < 150^\circ C$. $T_{j(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - SMALL-SIGNAL CURRENT GAIN

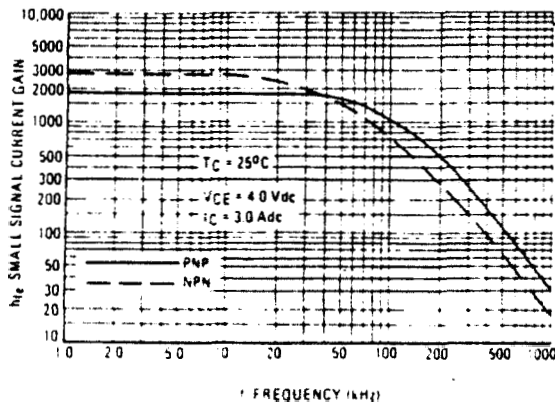
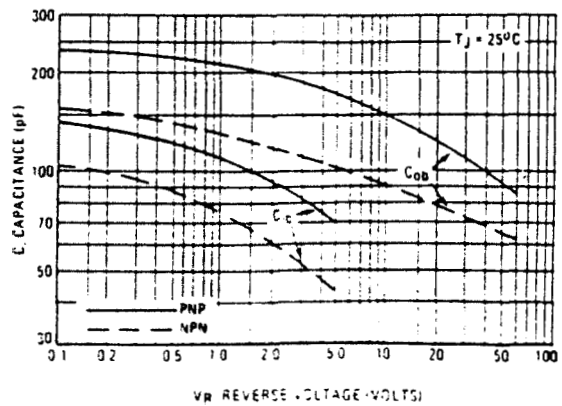
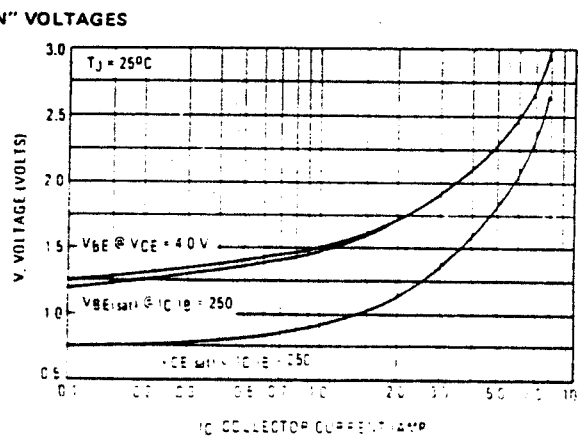
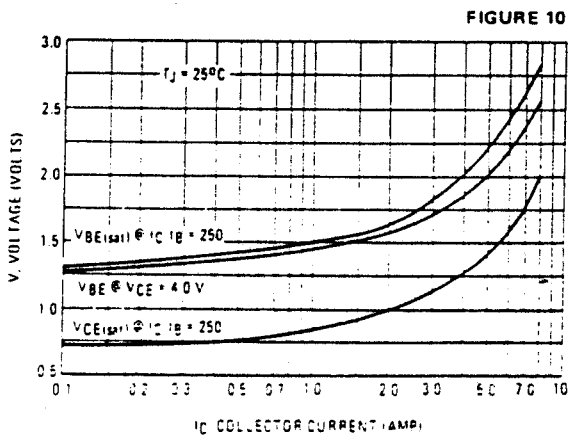
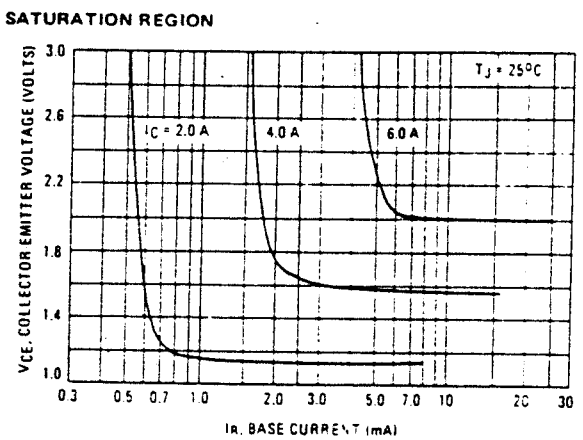
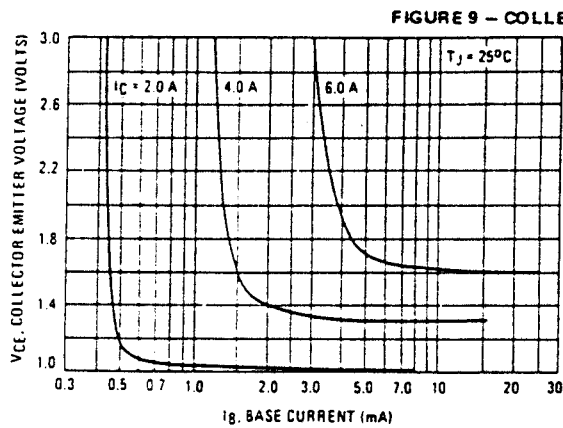
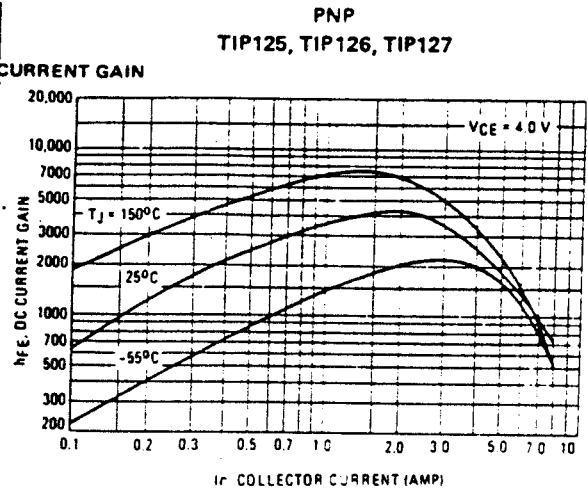
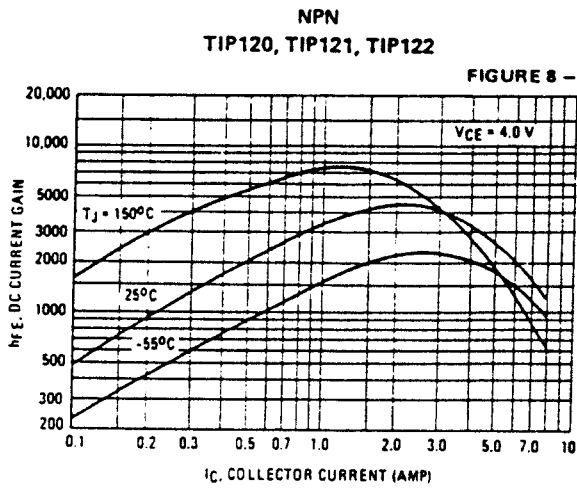


FIGURE 7 - CAPACITANCE



TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP



TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP

NPN
TIP120, TIP121, TIP122

PNP
TIP125, TIP126, TIP127

FIGURE 11 - TEMPERATURE COEFFICIENTS

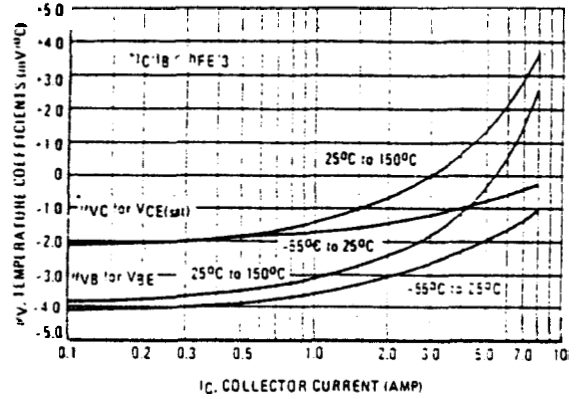
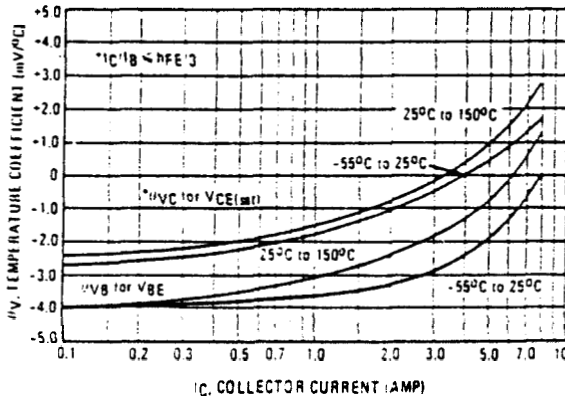


FIGURE 12 - COLLECTOR CUT-OFF REGION

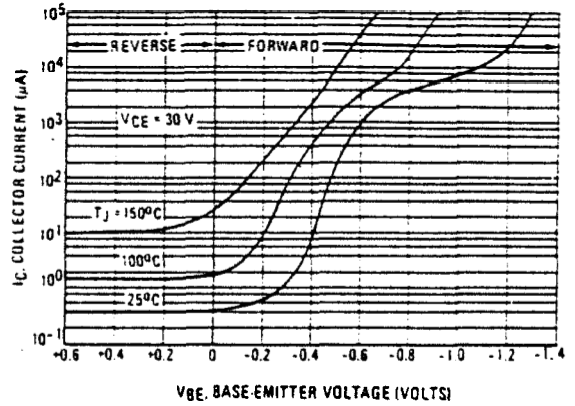
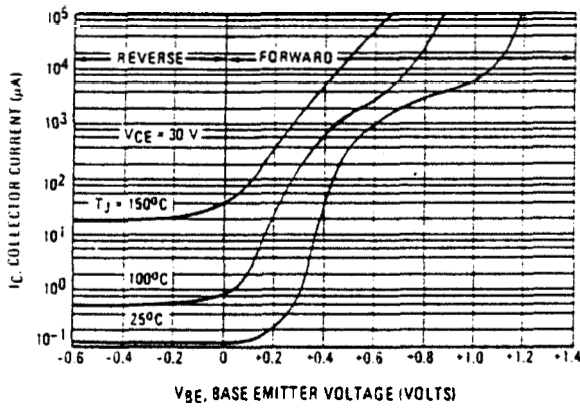
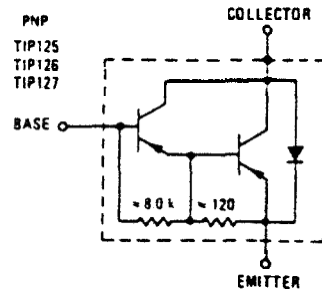
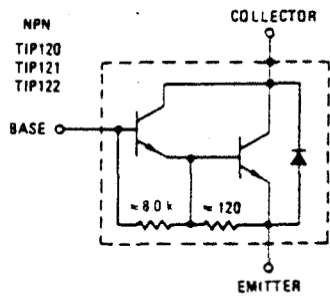


FIGURE 13 - DARLINGTON SCHEMATIC





MC14046B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in} . Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out} , and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1A$, $C1B$, $R1$, and $R2$. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh , when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- VCO Frequency = 1.4 MHz Typical @ $V_{DD} = 10$ Vdc
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ $V_{DD} = 10$ Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation – 70 μ W Typical @ $f_0 = 10$ kHz, $V_{DD} = 5.0$ Vdc, $R1 = 1.0$ M Ω , $R2 = \infty$, $R_{SF} = \infty$
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046B



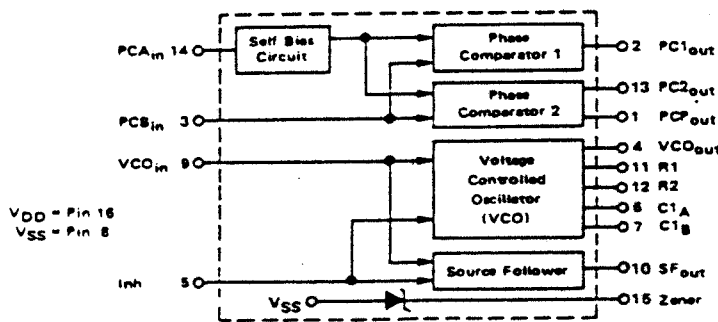
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package
	A	Extended Operating Temperature Range
	C	Limited Operating Temperature Range

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

MC14046B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device	T _A	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
	"1" Level V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage [#] (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	
		15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	
		15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device) (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	mAdc
		5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	
		10	-0.62	-	-0.5	-0.9	-	-0.35	-	
	Sink I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	
		15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (CL/CP Device) (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	mAdc
		5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
		10	-0.5	-	-0.4	-0.9	-	-0.3	-	
	Sink I _{OL}	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc
		10	1.3	-	1.1	2.25	-	0.9	-	
		15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP Device)	I _{in}	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device) (Per Package) (I _{nh} = "1" and PCA = "1")	I _{DD}	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
		10	-	10	-	0.010	10	-	300	
		15	-	20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device) (Per Package) (I _{nh} = "1" and PCA = "1")	I _{DD}	5.0	-	20	-	0.005	20	-	150	μAdc
		10	-	40	-	0.010	40	-	300	
		15	-	80	-	0.015	80	-	600	
Total Supply Current I _T (I _{nh} = "0", f _o = 10 kHz, C _L = 50 pF, R ₁ = 1 MΩ, R ₂ = ∞, R _{SF} = ∞, and 50% Duty Cycle)	I _T	5.0	I _T = (1.46 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (2.91 μA/kHz) f + I _{DD}							
		15	I _T = (4.37 μA/kHz) f + I _{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To Calculate Total Current in General:

$$I_T = 2.2 \times V_{DD} \left(\frac{V_{COin} - 1.65}{R_1} + \frac{V_{DD} - 1.35}{R_2} \right)^{3/4} + 1.6 \times \left(\frac{V_{COin} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f + 1 \times 10^{-1} V_{DD}^2 \left(\frac{100 - \% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_{DD}$$

where: I_T in μA, C_L in pF, V_{COin}, V_{DD} in Vdc, f in KHz, and R₁, R₂, R_{SF} in MΩ, C_L on V_{COout}.

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ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dc}	Minimum		Typical All Types	Maximum		Units
			AL Device	CL/CP Device		AL Device	CL/CP Device	
Output Rise Time †TLH = (3.0 ns/pF) C _L + 30 ns †TLH = (1.5 ns/pF) C _L + 15 ns †TLH = (1.1 ns/pF) C _L + 10 ns	†TLH	5.0 10 15	- - -	- - -	180 90 65	350 150 110	400 200 160	ns
Output Fall Time †THL = (1.5 ns/pF) C _L + 25 ns †THL = (0.75 ns/pF) C _L + 12.5 ns †THL = (0.55 ns/pF) C _L + 9.5 ns	†THL	5.0 10 15	- - -	- - -	100 50 37	175 75 55	200 100 80	ns

PHASE COMPARATORS 1 and 2

Input Resistance – PCA _{in}	R _{in}	5.0	1.0	1.0	2.0	-	-	MΩ
		10	0.2	0.2	0.4	-	-	
		15	0.1	0.1	0.2	-	-	
- PCB _{in}	R _{in}	15	150	15	1500	-	-	MΩ
Minimum Input Sensitivity AC Coupled – PCA _{in} C series = 1000 pF, f = 50 kHz	V _{in}	5.0	-	-	200	300	400	mV p-p
		10	-	-	400	600	800	
		15	-	-	700	1050	1400	
DC Coupled – PCA _{in} , PCB _{in}	-	5 to 15	See Noise Immunity					

VOLTAGE CONTROLLED OSCILLATOR (VCO)

Maximum Frequency (VCO _{in} = V _{DD} , C ₁ = 50 pF, R ₁ = 5 kΩ, and R ₂ = ∞)	f _{max}	5.0	0.50	0.35	0.70	-	-	MHz
		10	1.0	0.7	1.4	-	-	
		15	1.4	1.0	1.9	-	-	
Temperature – Frequency Stability (R ₂ = ∞)	-	5.0	-	-	0.12	-	-	%/°C
		10	-	-	0.04	-	-	
		15	-	-	0.015	-	-	
Linearity (R ₂ = ∞) (VCO _{in} = 2.50 V ± 0.30 V, R ₁ > 10 kΩ) (VCO _{in} = 5.00 V ± 2.50 V, R ₁ > 400 kΩ) (VCO _{in} = 7.50 V ± 5.00 V, R ₁ > 1000 kΩ)	-	5.0	-	-	1	-	-	%
		10	-	-	1	-	-	
		15	-	-	1	-	-	
Output Duty Cycle	-	5 to 15	-	-	50	-	-	%
Input Resistance – VCO _{in}	R _{in}	15	150	15	1500	-	-	MΩ

SOURCE-FOLLOWER

Offset Voltage (VCO _{in} minus SF _{out} , R _{SF} > 50 kΩ)	-	5.0	-	-	1.65	2.2	2.5	V _{dc}
		10	-	-	1.65	2.2	2.5	
		15	-	-	1.65	2.2	2.5	
Linearity (VCO _{in} = 2.50 V ± 0.30 V, R _{SF} > 50 kΩ) (VCO _{in} = 5.00 V ± 2.50 V, R _{SF} > 50 kΩ) (VCO _{in} = 7.50 V ± 5.00 V, R _{SF} > 50 kΩ)	-	5.0	-	-	0.1	-	-	%
		10	-	-	0.6	-	-	
		15	-	-	0.8	-	-	

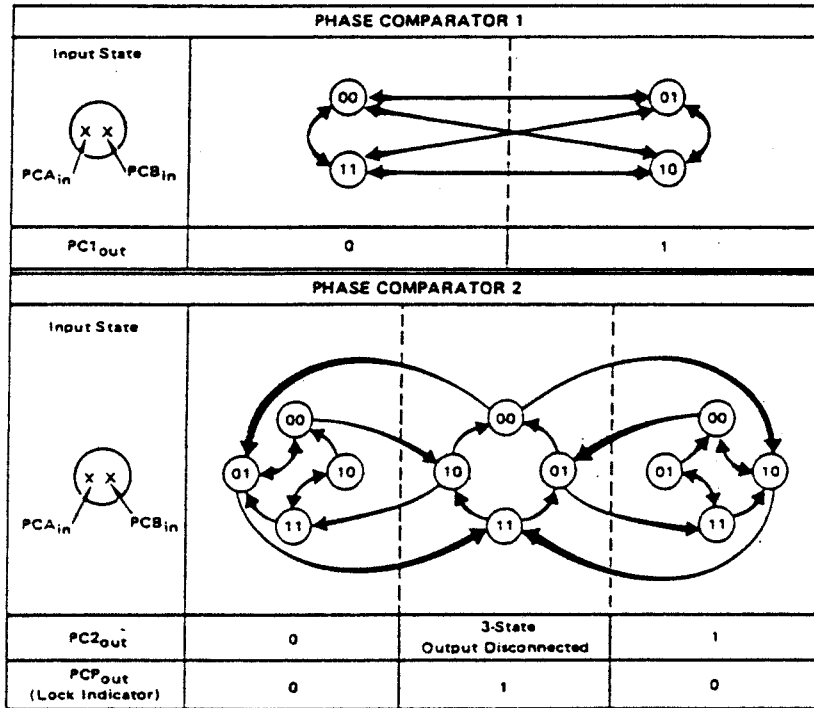
ZENER DIODE

Zener Voltage (I _Z = 50 μA)	V _Z	-	6.7	6.3	7.0	7.3	7.7	V _{dc}
Dynamic Resistance (I _Z = 1 mA)	R _Z	-	-	-	100	-	-	Ω

*The formula given is for the typical characteristics only.

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FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS



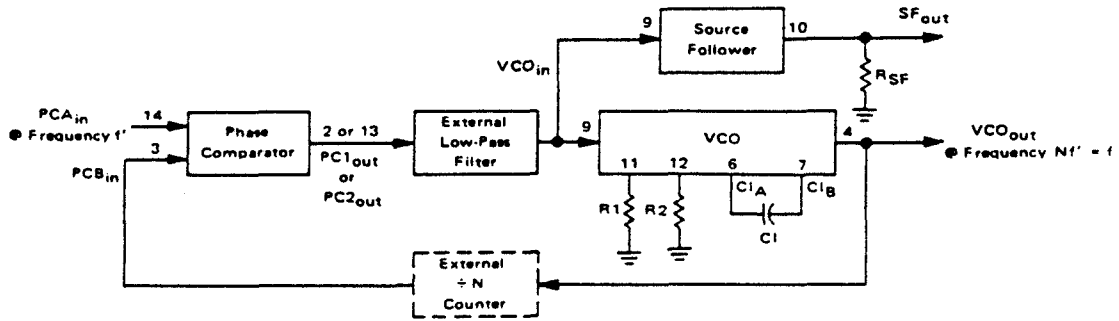
Refer to Waveforms in Figure 3.

FIGURE 2 – DESIGN INFORMATION

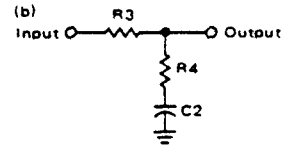
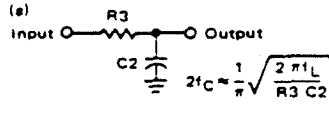
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA _{in} .	VCO in PLL system adjusts to center frequency (f ₀).	VCO in PLL system adjusts to minimum frequency (f _{min}).
Phase angle between PCA _{in} and PCB _{in} .	90° at center frequency (f ₀), approaching 0° and 180° at ends of lock range (2f _L).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f _L).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. 2f _L = full VCO frequency range = f _{max} - f _{min} .	
Capture frequency range (2f _C).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f _C < f _L	f _C = f _L
Center frequency (f ₀).	The frequency of VCO _{out} , when VCO _{in} = 1/2 VDD	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \quad (\text{VCO input} = V_{SS})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \quad (\text{VCO input} = V_{DD})$ <p>Where: 10K < R₁ < 1M 10K < R₂ < 1M 100pF < C₁ < .01 μF</p>	

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FIGURE 3 - GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi \Delta f}$$

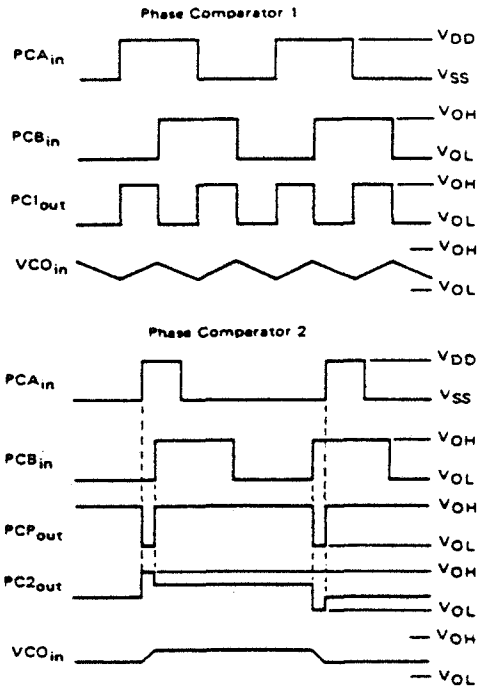
$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{max}^2} - R_4 C_2$$

$$\Delta f = f_{max} - f_{min}$$

Note: for further information, see:

- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.

Waveforms



CA3130, CA3130A, CA3130B Types

BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

RCA-CA3130T, CA3130E, CA3130S, CA3130AT, CA3130AS, CA3130AE, CA3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ± 2.5 to ± 8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications

requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix). All types operate over the full military-temperature range of -55°C to $+125^{\circ}\text{C}$. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of -55°C to $+125^{\circ}\text{C}$. The CA3130A offers superior input characteristics over those of the CA3130.

Features:

- MOS/FET input stage provides:
 - very high $Z_i = 1.5 \text{ T}\Omega$ ($1.5 \times 10^{12} \Omega$) typ.
 - very low $I_i = 5 \text{ pA}$ typ. at 15-V operation
 - 2 pA typ. at 5-V operation
 - Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
 - COS/MOS output stage permits signal swing to either (or both) supply rails
- } Ideal for single-supply applications
- Low V_{IO} : 2 mV max. (CA3130B)
 - Wide BW: 15 MHz typ. (unity-gain crossover)
 - High SR: 10 V/ μs typ. (unity-gain follower)
 - High output current (I_O): 20 mA typ.
 - High A_{OL} : 320,000 (110 dB) typ.
 - Compensation with single external capacitor
- #### Applications:
- Ground-referenced single-supply amplifiers
 - Fast sample-and-hold amplifiers
 - Long-duration timers/monostables
 - High-input-impedance comparators (ideal interface with digital COS/MOS)
 - High-input-impedance wideband amplifiers
 - Voltage followers (e.g., follower for single-supply D/A converter)
 - Voltage regulators (permits control of output voltage down to zero volts)
 - Peak detectors
 - Single-supply full-wave precision rectifiers
 - Photo-diode sensor amplifiers

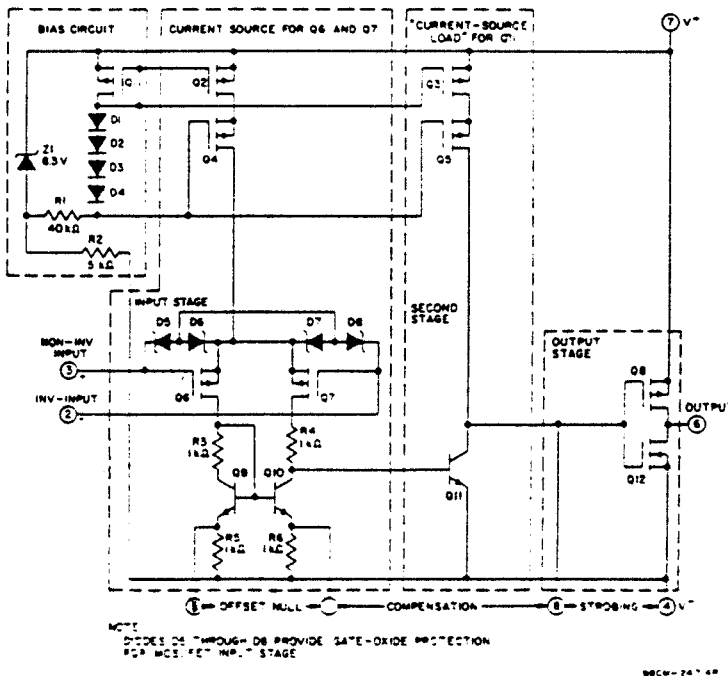


Fig. 1 - Schematic diagram of the CA3130 Series

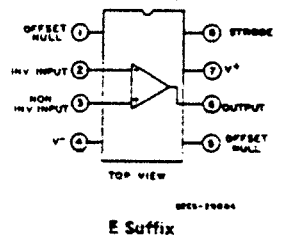
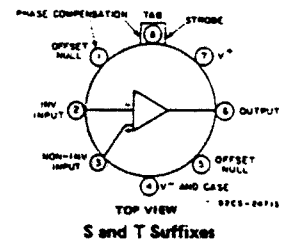


Fig. 2 - Functional diagrams for the CA3130 series.

CA3130, CA3130A, CA3130B Types

MAXIMUM RATINGS, Absolute-Maximum Values

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals) 16 V
 DIFFERENTIAL MODE INPUT VOLTAGE ± 3 V
 COMMON-MODE DC INPUT VOLTAGE... (V $^+$ +8 V) to (V $^-$ -0.5 V)
 INPUT-TERMINAL CURRENT 1 mA
 DEVICE DISSIPATION: WITHOUT HEAT SINK -
 UP TO 55°C 830 mW
 ABOVE 55°C Derate linearly 6.67 mW/°C
 WITH HEAT SINK -
 AT 125°C 418 mW
 BELOW 125°C Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
 OPERATING (all types) -55 to +125°C
 STORAGE (all types) -65 to +150°C
 OUTPUT SHORT-CIRCUIT DURATION INDEFINITE
 LEAD TEMPERATURE (DURING SOLDERING): AT DISTANCE 1/16 \pm 1/32 INCH (1.59 \pm 0.79 mm) FROM CASE FOR 10 SECONDS MAX. +265°C

*Short circuit may be applied to ground or to either supply.

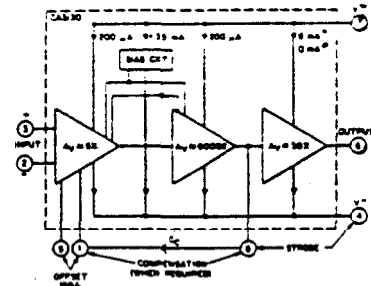


Fig. 3 - Block diagram of the CA3130 Series.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V^+ = 15\text{ V}$, $V^- = 0\text{ V}$ (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units	
	CA3130B (T,S)			CA3130A (T,S,E)			CA3130 (T,S,E)				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Offset Voltage, $ V_{IO} $, $V^{\pm} = \pm 7.5\text{ V}$	-	0.8	2	-	2	5	-	8	15	mV	
Input Offset Current, $ I_{IO} $, $V^{\pm} = \pm 7.5\text{ V}$	-	0.5	10	-	0.5	20	-	0.5	30	pA	
Input Current, I_I , $V^{\pm} = \pm 7.5\text{ V}$	-	5	20	-	5	30	-	5	50	pA	
Large-Signal Voltage Gain, A_{OL} , $V_O = 10\text{ V}_{D-D}$, $R_L = 2\text{ k}\Omega$	100 k	320 k	-	50 k	320 k	-	50 k	320 k	-	V/V	
	100	110	-	94	110	-	94	110	-	dB	
Common-Mode Rejection Ratio, CMRR	86	100	-	80	90	-	70	90	-	dB	
Common-Mode Input Voltage Range, V_{ICR}	0	-0.5 to 12	10	0	-0.5 to 12	10	0	-0.5 to 12	10	V	
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$, $V^{\pm} = \pm 7.5\text{ V}$	-	32	100	-	32	150	-	32	320	$\mu\text{V/V}$	
Maximum Output Voltage:											
At $R_L = 2\text{ k}\Omega$	V_{OM}^+	12	13.3	-	12	13.3	-	12	13.3	-	V
	V_{OM}^-	-	0.002	0.01	-	0.002	0.01	-	0.002	0.01	
At $R_L = \infty$	V_{OM}^+	14.99	15	-	14.99	15	-	14.99	15	-	V
	V_{OM}^-	-	0	0.01	-	0	0.01	-	0	0.01	
Maximum Output Current:											
I_{OM}^+ (Source) @ $V_O = 0\text{ V}$	12	22	45	12	22	45	12	22	45	mA	
I_{OM}^- (Sink) @ $V_O = 15\text{ V}$	12	20	45	12	20	45	12	20	45		
Supply Current, I^+ , $V_O = 7.5\text{ V}$, $R_L = \infty$											
$V_O = 0\text{ V}$, $R_L = \infty$	-	10	15	-	10	15	-	10	15	mA	
	-	2	3	-	2	3	-	2	3		
Input Current, I_I^+	-	Fig.12	15	-	Fig.12	-	-	Fig.12	-	nA	
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T^{\circ}$	-	5	15	-	10	-	-	10	-	$\mu\text{V}/^{\circ}\text{C}$	
Large-Signal Voltage Gain, A_{OL}^*	50 k	320 k	-	-	320 k	-	-	320 k	-	dB	
	94	110	-	-	110	-	-	110	-		

* $T_A = -55$ to $+125^\circ\text{C}$, $V^{\pm} = \pm 7.5\text{ V}$ (I_I and $\Delta V_{IO}/\Delta T$), $V_O = 10\text{ V}_{D-D}$ and $R_L = 2\text{ k}\Omega$ (A_{OL}).

Fig. 3 - Block diagram of the CA3130 Series.

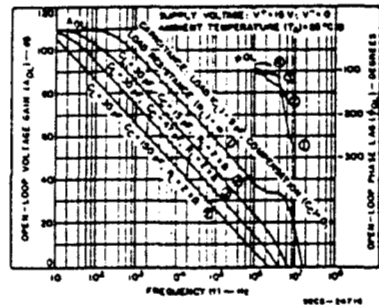


Fig. 4 - Open-loop voltage gain and phase shift vs. frequency for various values of C_L , C_O and R_L .

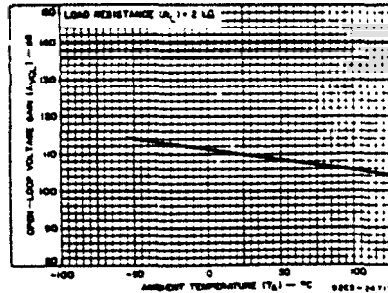


Fig. 5 - Open-loop gain vs. temperature.

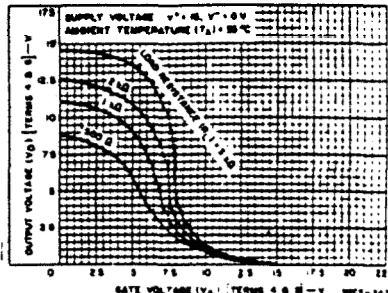


Fig. 6 - Voltage transfer characteristics of COS/MOS output stage.

CA3130, CA3130A, CA3130B Types

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
	$V^+ = +7.5\text{ V}$ $V^- = -7.5\text{ V}$ $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)				
Input Offset Voltage Adjustment Range	10 k Ω across Terms. 4 and 5 or 4 and 1	± 22	± 22	± 22	mV
Input Resistance, R_I		1.5	1.5	1.5	T Ω
Input Capacitance, C_I	$f = 1\text{ MHz}$	4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	$BW = 0.2\text{ MHz}$ $R_S = 1\text{ M}\Omega^*$	23	23	23	μV
Unity Gain Crossover Frequency, f_T	$C_C = 0$	15	15	15	MHz
	$C_C = 47\text{ pF}$	4	4	4	
Slew Rate, SR:	Open Loop $C_C = 0$	30	30	30	V/ μs
	Closed Loop $C_C = 56\text{ pF}$	10	10	10	
Transient Response: Rise Time, t_r	$C_C = 56\text{ pF}$ $C_L = 25\text{ pF}$ $R_L = 2\text{ k}\Omega$	0.09	0.09	0.09	μs
	Overshoot	10	10	10	%
Settling Time (4 V_{p-p} Input to $<0.1\%$)	(Voltage Follower)	1.2	1.2	1.2	μs

* Although a 1-M Ω source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 M Ω .

CHARACTERISTIC	TEST CONDITIONS	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
	$V^+ = 5\text{ V}$ $V^- = 0\text{ V}$ $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)				
Input Offset Voltage, V_{IO}		1	2	8	mV
Input Offset Current, I_{IC}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage Gain, A_{OL}	$V_O = 4\text{ V}_{p-p}$ $R_L = 5\text{ k}\Omega$	100 k	100 k	100 k	V/V
		100	100	100	
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	$V_O = 5\text{ V}$ $R_L = \infty$	300	300	300	μA
	$V_O = 2.5\text{ V}$ $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	$\mu\text{V/V}$

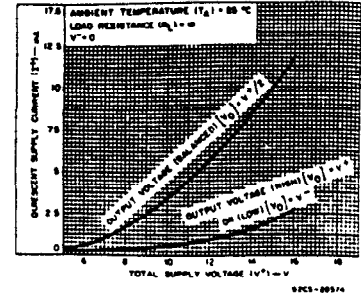


Fig. 7 - Quiescent supply current vs. supply voltage.

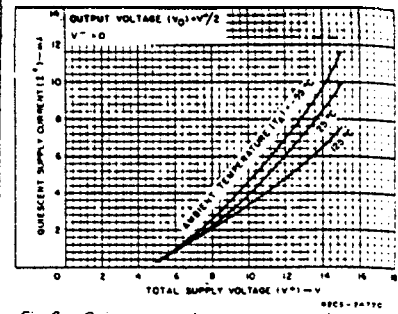


Fig. 8 - Quiescent supply current vs. supply voltage at several temperatures.

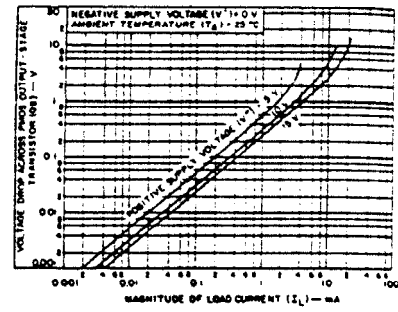


Fig. 9 - Voltage across PMOS output transistor (Q8) vs. load current.

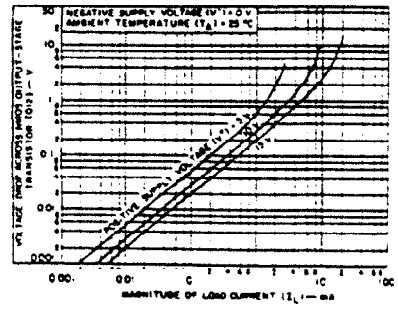


Fig. 10 - Voltage across NMOS output transistor (Q2) vs. load current.

CA3130, CA3130A, CA3130B Types

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for

PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 3.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical ohm loads are readily driven by the output stage. Because large-signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at $T_A = 25^\circ\text{C}$ when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 11 contains data showing the variation of input current as a function of common-mode input voltage at $T_A = 25^\circ\text{C}$. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the

gate-protection diodes in the input circuit and, therefore, a function of the applied

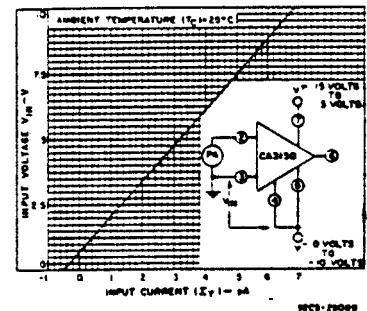


Fig. 11 — Input current vs. common-mode voltage.

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C . The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

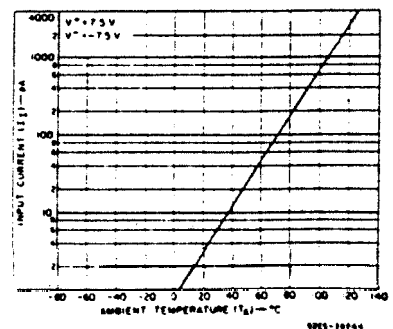


Fig. 12 — Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in

†For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3800E "COS/MOS Transistor Array".

CA3130, CA3130A, CA3130B Types

current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig. 13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

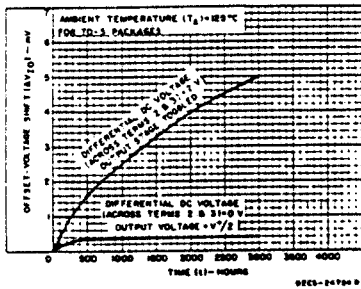


Fig. 13 - Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the

negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μ V when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source

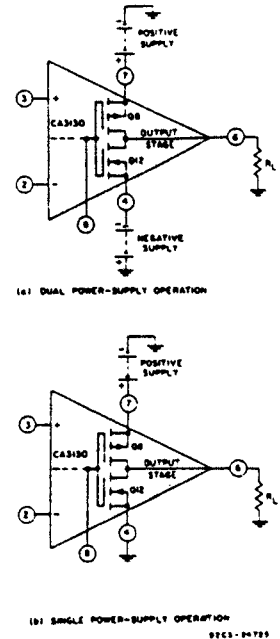


Fig. 14 - CA3130 output stage in dual and single power-supply operation.

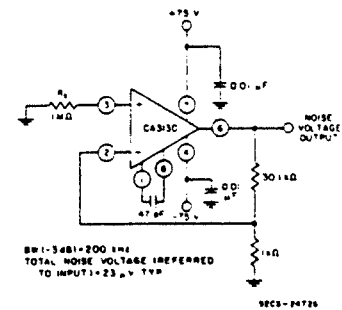


Fig. 15 - Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



MC14538B

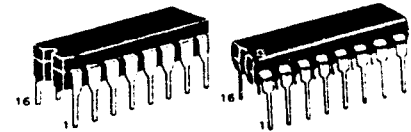
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X . Linear CMOS techniques allow more precise control of output pulse width.

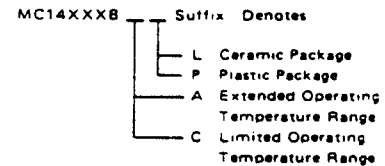
- $\pm 1.0\%$ Typical Pulsewidth Variation from Part to Part
- $\pm 0.5\%$ Typical Pulsewidth Variation over Temperature Range
- New Formula: $T = RC$ (T in seconds, R in ohms, C in farads)
- Pulse Width Range = $10 \mu s$ to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5.0 nA/package typical @ 5 Vdc
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative-Going Edge
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- For Pulse Widths Less Than $10 \mu s$ the MC14528B is Recommended



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION



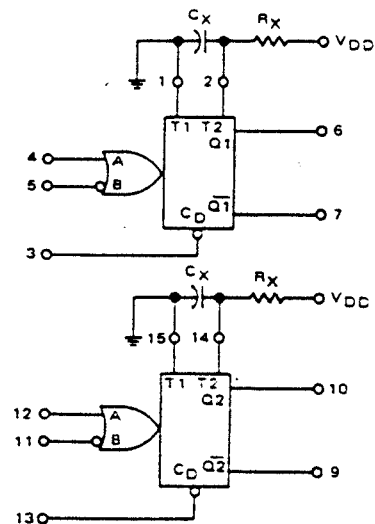
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device	T_A	-55 to +125	$^{\circ}C$
Operating Temperature Range - CL/CP Device		-40 to +85	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
 V_{SS} = Pin 8, Pin 1, Pin 15

MC14538B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit	
			Min	Max	Min	Typ	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage# (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mA _{dc}	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
	Sink I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mA _{dc}	
		10	1.6	-	1.3	2.25	-	0.9	-		
		15	4.2	-	3.4	8.8	-	2.4	-		
Output Drive Current (CL/CP Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	mA _{dc}	
		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-		
		10	-1.3	-	-1.1	-2.25	-	-0.9	-		
	Sink I _{OL}	5.0	0.52	-	0.44	0.88	-	0.36	-	mA _{dc}	
		10	1.3	-	1.1	2.25	-	0.9	-		
		15	3.6	-	3.0	8.8	-	2.4	-		
Input Current, Pin 2 or 14	I _{in}	15	-	±0.02	-	±0.00001	±0.05	-	±0.5	μA _{dc}	
Input Current, Other Inputs (AL Device)	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μA _{dc}	
Input Current, Other Inputs (CL/CP Device)	I _{in}	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μA _{dc}	
Input Capacitance, Pin 2 or 14	C _{in}	-	-	-	-	25	-	-	-	pF	
Input Capacitance, Other Inputs (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	-	5.0	-	0.005	5.0	-	150	μA _{dc}	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	-	20	-	0.005	20	-	150	μA _{dc}	
		10	-	40	-	0.010	40	-	300		
		15	-	80	-	0.015	80	-	600		
Quiescent Current, Active State (Q1 = Logic 1) (Q2 = Logic 0)	I _{DD}	5.0	-	-	-	35	-	-	-	μA _{dc}	
		10	-	-	-	80	-	-	-		
		15	-	-	-	125	-	-	-		
**Total Supply Current at an external load capacitance (C _L) and at external timing network (R _X , C _X)	I _T	5.0 10.0 15.0	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ <p>where: I_T in μA (one monostable switching only), C_X in μF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.</p>								

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

MC14538B

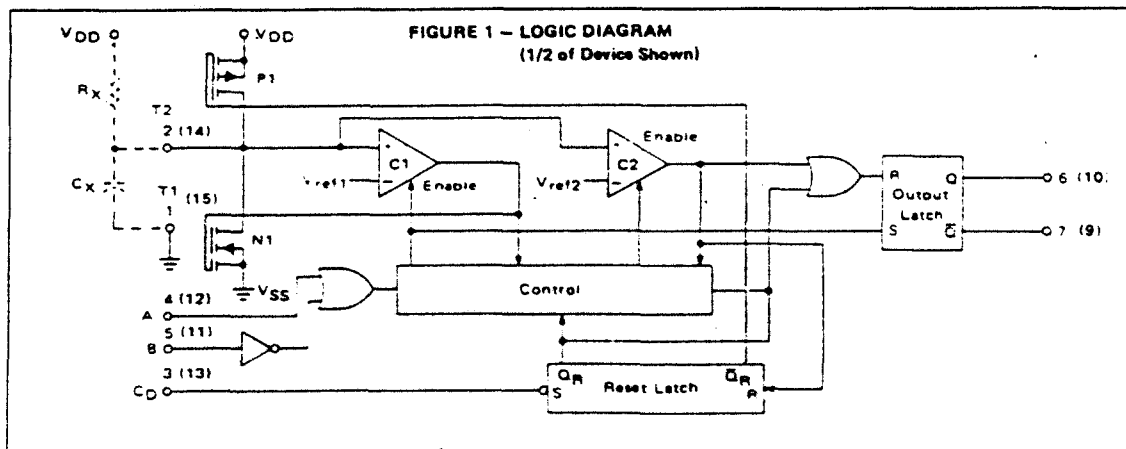
SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

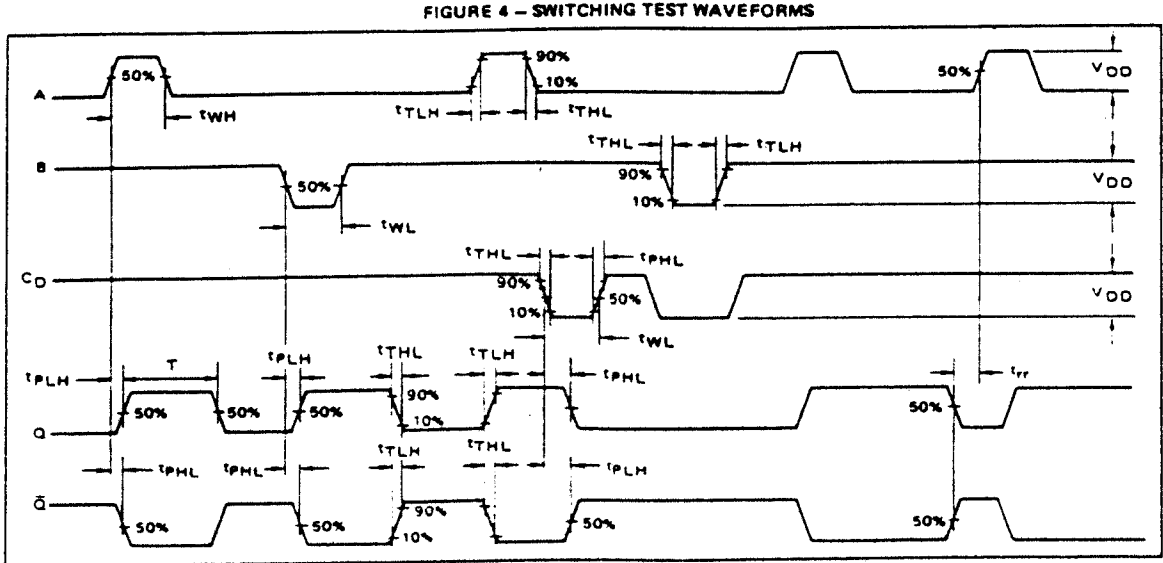
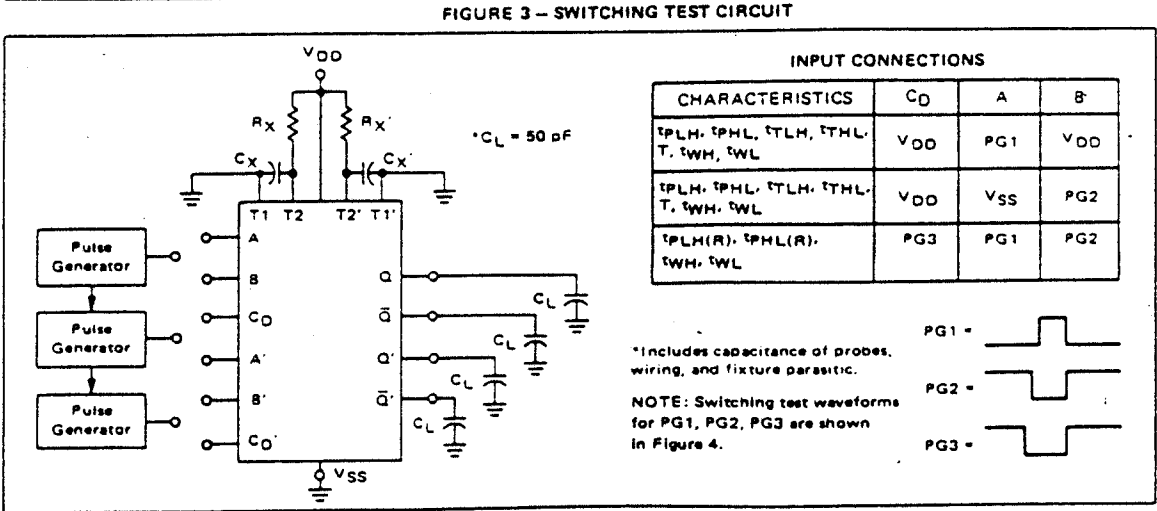
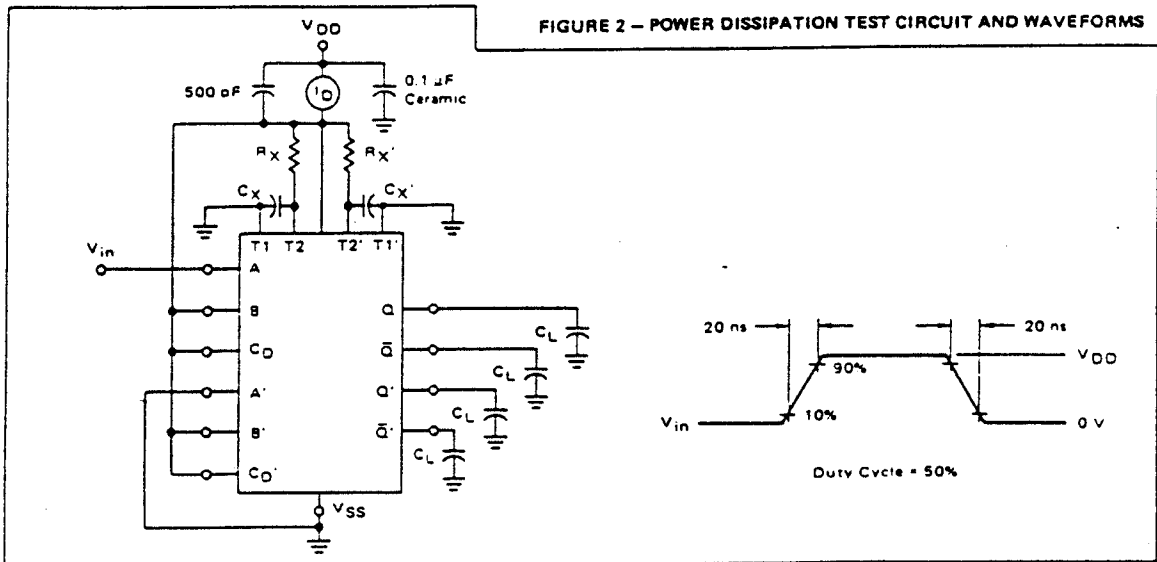
Characteristic	Symbol	V _{DD} V _{dc}	All Types			Unit
			Min	Typ	Max	
Output Rise Time t _{TLH} = (1.35 ns/pF) C _L + 33 ns t _{TLH} = (0.60 ns/pF) C _L + 20 ns t _{TLH} = (0.40 ns/pF) C _L + 20 ns	t _{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time t _{THL} = (1.35 ns/pF) C _L + 33 ns t _{THL} = (0.60 ns/pF) C _L + 20 ns t _{THL} = (0.40 ns/pF) C _L + 20 ns	t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or \bar{Q} t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 255 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 132 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 97 ns C _D to Q or \bar{Q} t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 205 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 107 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 82 ns	t _{PLH} , t _{PHL}	5.0 10 15 5.0 10 15	— — — — — —	300 150 100 250 125 95	600 300 220 500 250 190	ns
Minimum Input Pulse Width A, B or C _D	t _{WH} , t _{WL}	5.0 10 15	— — —	35 30 25	70 60 50	ns
Minimum Retrigger Time	t _{rr}	5.0 10 15	0 0 0	— — —	— — —	ns
Output Pulse Width — Q or \bar{Q} Refer to Figure 9 for other values of R _X and C _X . C _X = 0.002 μF, R _X = 100 kΩ C _X = 0.1 μF, R _X = 100 kΩ C _X = 10 μF, R _X = 100 kΩ	T	5.0 10 15 5.0 10 15 5.0 10 15	— 210 212 214 9.3 9.5 9.6 0.915 0.93 0.94	— 222 224 226 9.86 10 10.14 0.965 0.98 0.99	— 234 236 238 10.4 10.5 10.7 1.015 1.03 1.04	μs ms s
Pulse Width Match between circuits in the same package. C _X = 0.1 μF, R _X = 100 kΩ	$\frac{100(T_1 - T_2)}{T_1}$	5.0 10 15	— — —	±1 ±1 ±1	— — —	%

OPERATING CONDITIONS

External Timing Resistance	R _X	—	5.0	—	*	kΩ
External Timing Capacitance	C _X	—	0	—	No Limit	pF

*The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance.





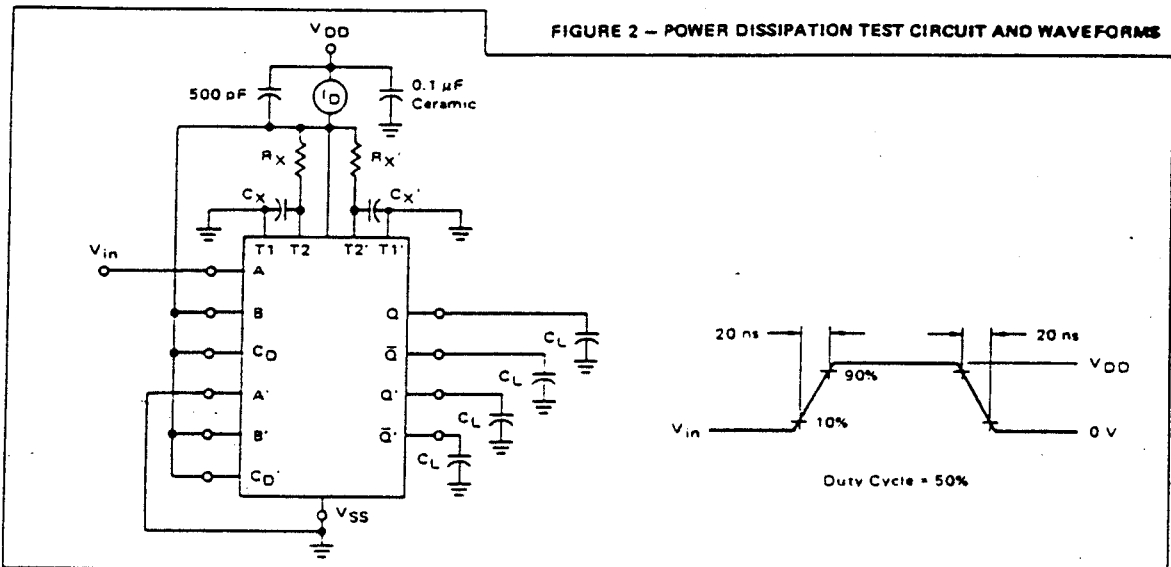


FIGURE 3 – SWITCHING TEST CIRCUIT

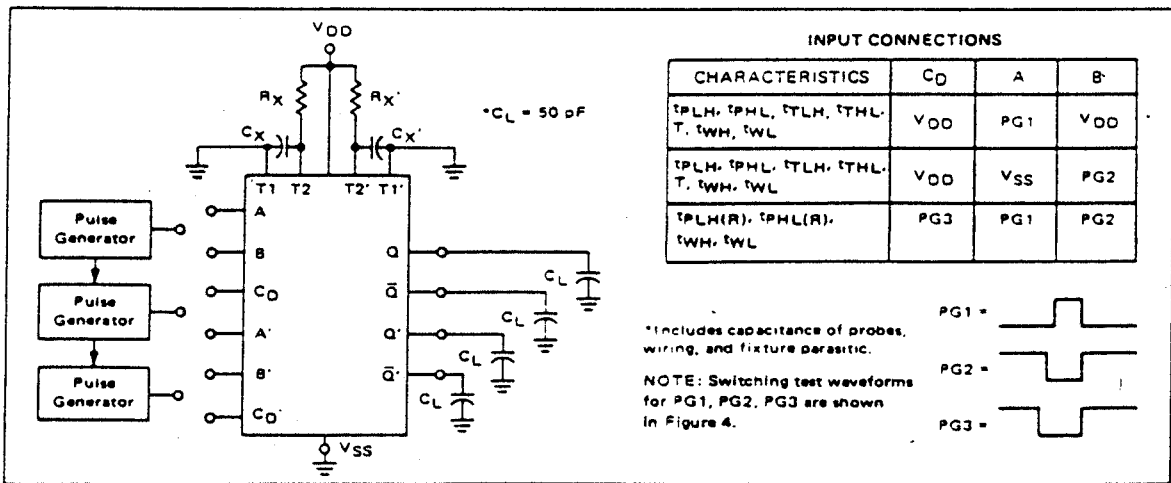
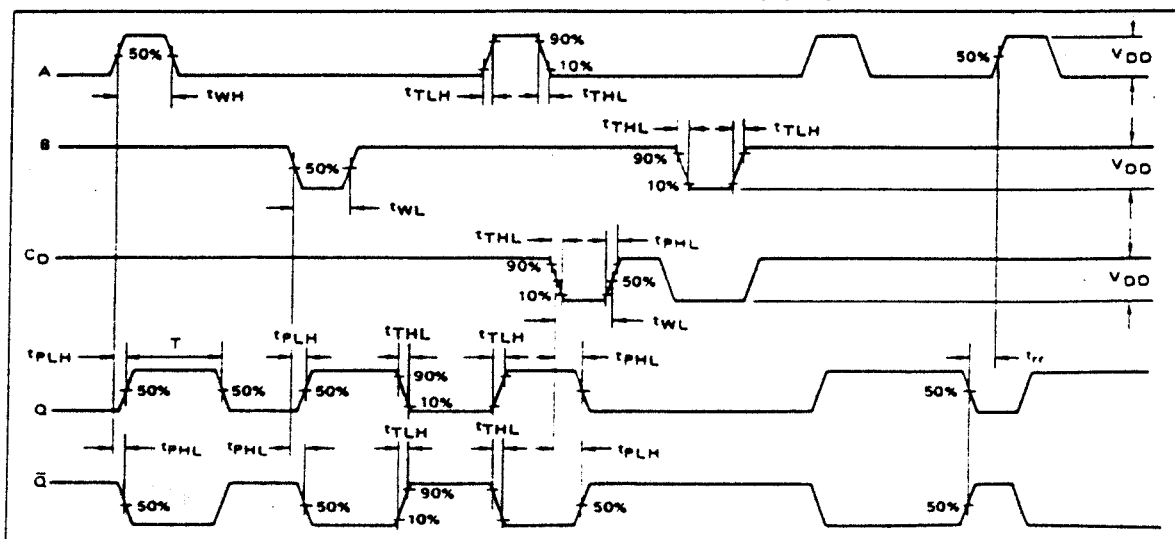


FIGURE 4 – SWITCHING TEST WAVEFORMS



MC14538B

FIGURE 5 – TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

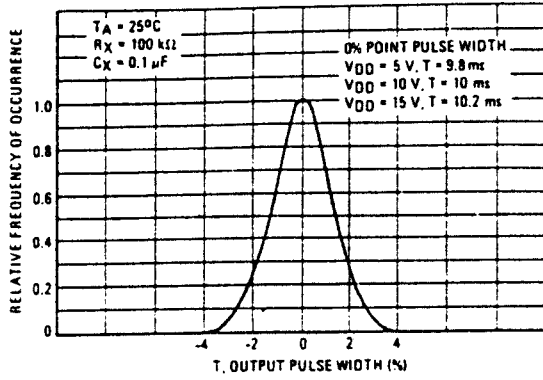


FIGURE 6 – TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE V_{DD}

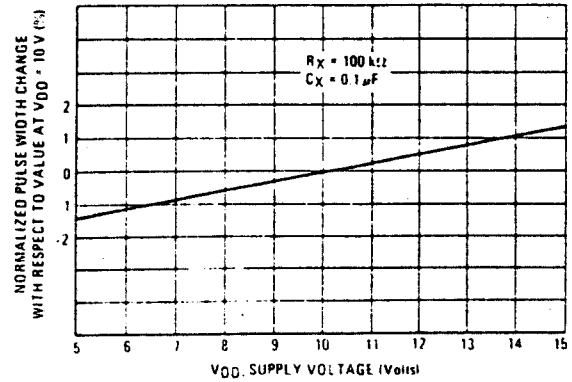


FIGURE 7 – TYPICAL TOTAL SUPPLY CURRENT versus OUTPUT DUTY CYCLE

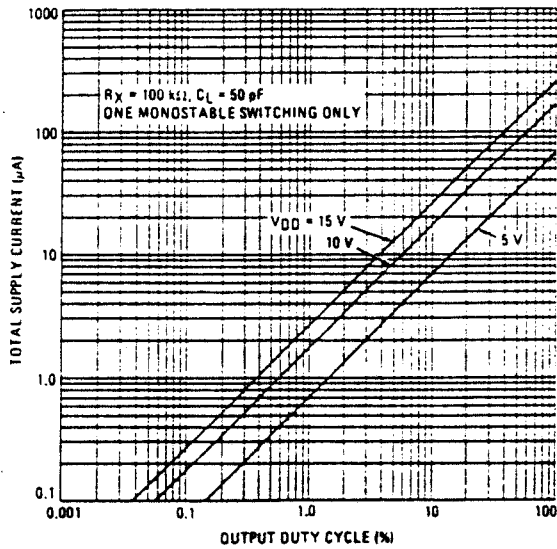


FIGURE 7 – TYPICAL PULSE WIDTH ERROR versus TEMPERATURE

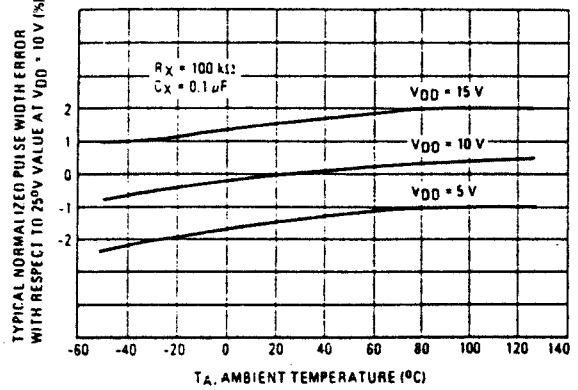
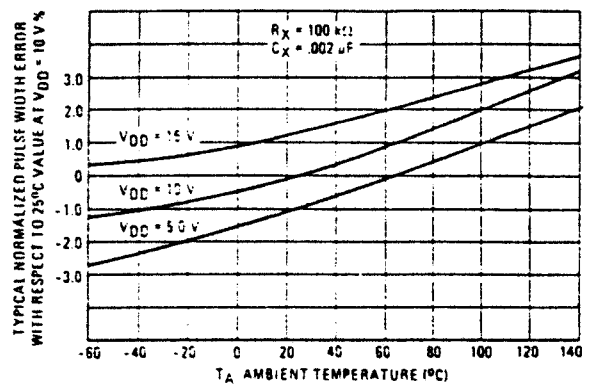
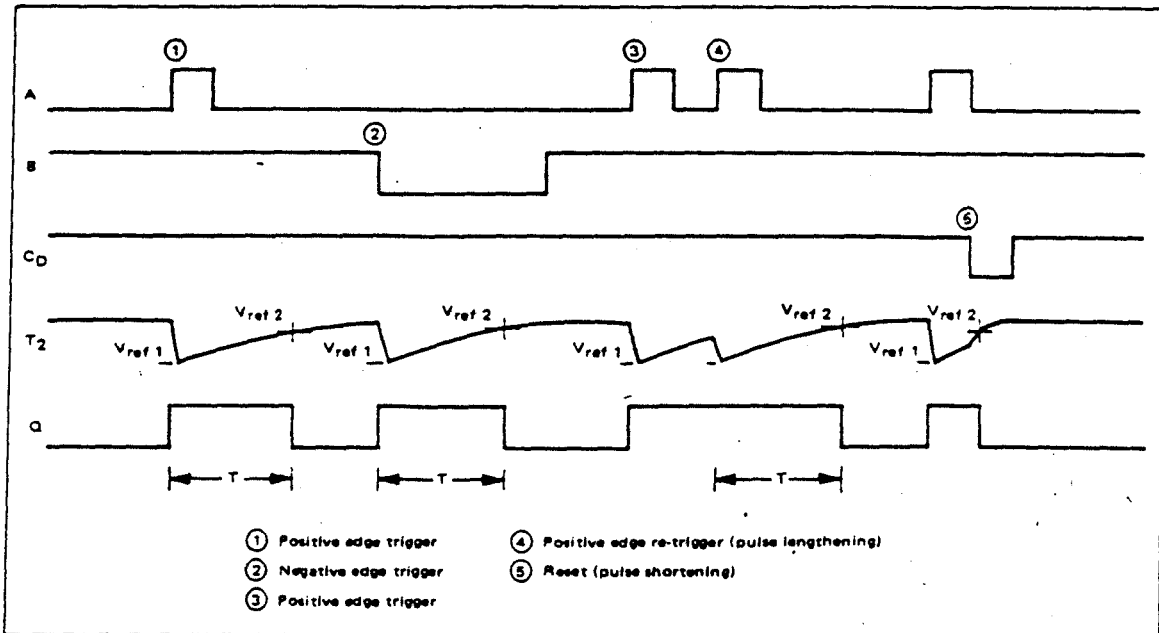


FIGURE 9 – TYPICAL PULSE WIDTH ERROR versus TEMPERATURE



THEORY OF OPERATION

FIGURE 10 – Timing Operation



TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_x completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 (1). At the same time the output latch is set. With transistor N1 on, the capacitor C_x rapidly discharges toward V_{SS} until V_{ref 1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_x begins to charge through the timing resistor, R_x, toward V_{DD}. When the voltage across C_x equals V_{ref 2}, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 (2). This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

It should be noted that in the quiescent state C_x is fully charged to V_{DD} causing the current through resistor R_x to be zero. Both comparators are "off" with the total

device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_x, R_x, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs (3) followed by another valid trigger (4) before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{ref 1}, but has not yet reached V_{ref 2}, will cause an increase in output pulse width T. When a valid retrigger is initiated (4), the voltage at T₂ will again drop to V_{ref 1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 (5). When the voltage on the capacitor reaches V_{ref 2}, the

MC14538B

reset latch will clear, and will then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and \bar{Q} outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B (or MC14528B) is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than $(V_{DD}) \cdot (C) / (10 \text{ mA})$. For example, if $V_{DD} = 10 \text{ V}$ and $C_x = 10 \mu\text{F}$, the V_{DD} supply should discharge no faster than $(10 \text{ V}) \times (10 \mu\text{F}) / (10 \text{ mA}) = 10 \text{ ms}$. This is normally not a problem since power supplies are heavily

filtered and cannot discharge at this rate.

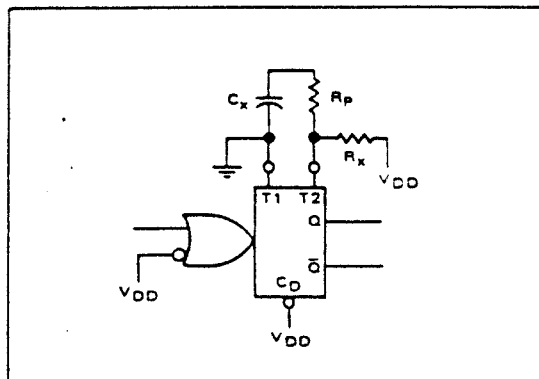
When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility, a protection resistor, R_p , can be placed between the capacitor C_x and pin 2 (or 14) of the device to limit the discharge current from the capacitor to the V_{DD} supply. Internally, the protection diode is equivalent to a diode and resistor connected in series between pin T2 and V_{DD} . The diode has a forward drop of 0.625 V and the resistance is about 250 Ω .

To limit the discharge current to 10 mA under conditions of instantaneous change of pin 16 from V_{DD} to V_{SS} , R_p is calculated from the equation:

$$R_p = \frac{(V_{DD} - 0.625\text{V})}{(0.010 \text{ Amp})} - 250 \Omega$$

The pulse width formula now changes from $T = R_x C_x$ to $T = (R_x + R_p) C_x$. Figure 11 demonstrates the proper connection of the protection resistor.

FIGURE 11 – Use of a Resistor to Limit Power Down Current Surge



TYPICAL APPLICATIONS

FIGURE 12 – Retriggerable Monostables Circuitry

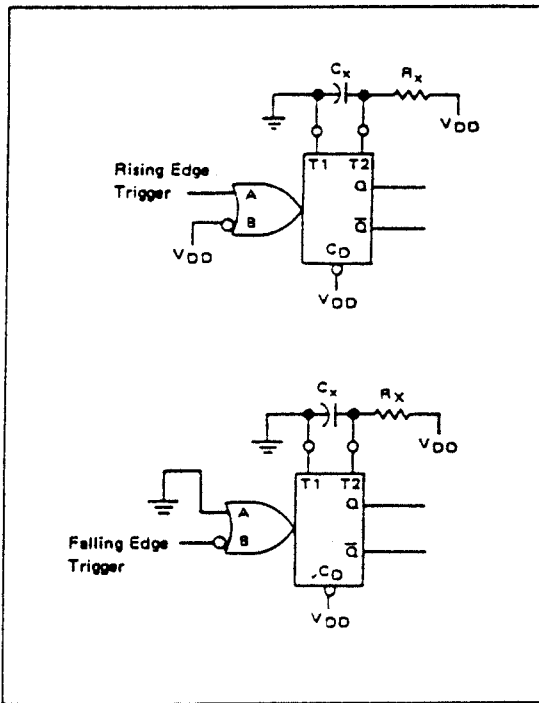


FIGURE 13 – Non-retriggerable Monostables Circuitry

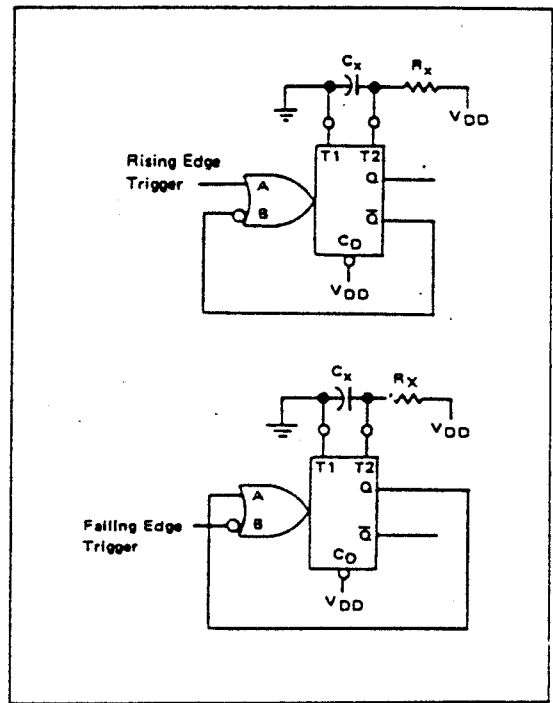


FIGURE 14 – Reduction of Power-Up Output Pulse Width

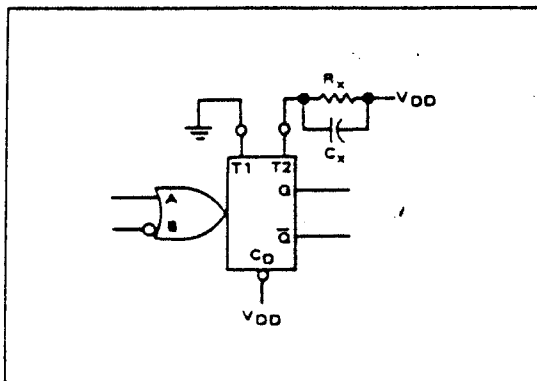
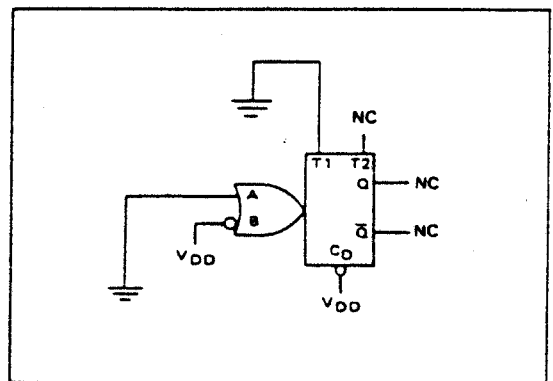


FIGURE 15 – Connection of Unused Sections





MC14049UB MC14050B

HEX BUFFERS

The MC14049UB hex inverter/buffer and MC14050B noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC} . The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters ($V_{CC} = 5.0\text{ V}$, $V_{OL} \leq 0.4\text{ V}$, $I_{OL} \geq 3.2\text{ mA}$). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

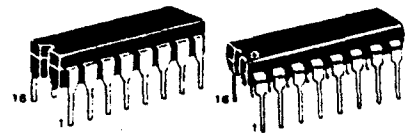
- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications—MC14049UB
Meets JEDEC B Specification—MC14050B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

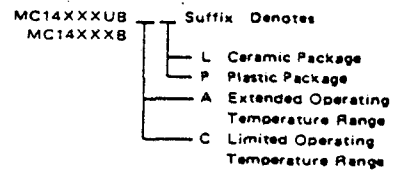
Inverting — MC14049UB
Noninverting — MC14050B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

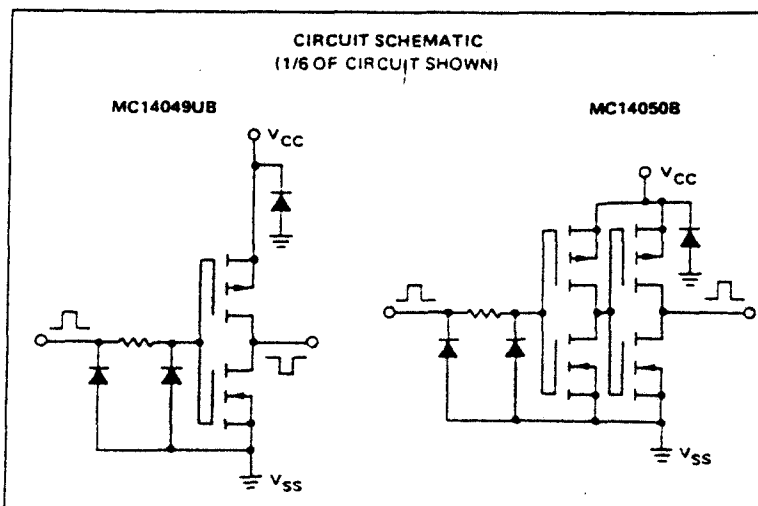
ORDERING INFORMATION



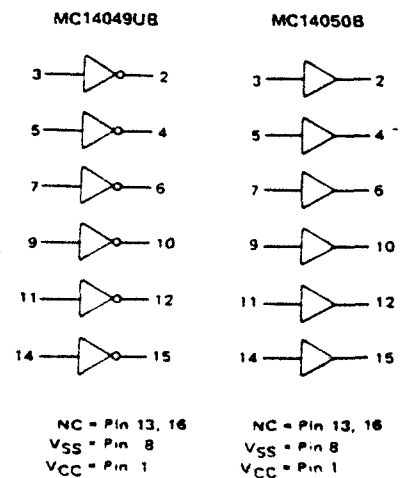
MAXIMUM RATINGS (Voltages referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to +18	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	45	mAdc
Operating Temperature Range — AL Device	T_A	-55 to +125	$^{\circ}\text{C}$
		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	VDD		25°C			Unit
		Vdc	Min	Max	Min	Typ	
Output Voltage VIN = VDD or 0	VOH	5.0	5.0	4.95	5.0	5.0	Vdc
	VOL	5.0	0	0.05	0	0.05	Vdc
Input Voltage #MCI4049UB (VO = 4.5 Vdc) (VO = 9.0 Vdc) (VO = 13.5 Vdc)	VOH	5.0	4.5	4.95	4.5	4.95	Vdc
	VIL	5.0	1.0	2.25	1.0	2.25	Vdc
Input Voltage #MCI14050B (VO = 0.5 Vdc) (VO = 1.0 Vdc) (VO = 1.5 Vdc)	VOH	5.0	0.5	0.95	0.5	0.95	Vdc
	VIL	5.0	1.5	2.25	1.5	2.25	Vdc
Input Voltage #MCI4050B (VO = 0.5 Vdc) (VO = 1.0 Vdc) (VO = 1.5 Vdc)	VOH	5.0	0.5	0.95	0.5	0.95	Vdc
	VIL	5.0	1.5	2.25	1.5	2.25	Vdc
Output Drive Current (AL Device) (VOH = 2.5 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vdc)	IOH	5.0	-1.6	-1.25	-2.5	-0.9	mADC
	IOL	5.0	3.75	3.2	6.0	5.2	mADC
Output Drive Current (CL/CP Device) (VOH = 2.5 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vdc)	IOH	5.0	-1.5	-1.25	-2.5	-1.0	mADC
	IOL	5.0	3.6	3.2	6.0	2.6	mADC
Sink (VOL = 0.4 Vdc) (VOL = 0.5 Vdc) (VOL = 1.5 Vdc)	IOS	5.0	3.6	3.2	6.0	2.6	mADC
	IOL	5.0	9.6	8.0	16	6.6	mADC
Source (VOH = 2.5 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vdc)	IOS	5.0	-1.5	-1.25	-2.5	-1.0	mADC
	IOH	5.0	-4.5	-3.75	-10	-3.0	mADC
Input Current (AL Device) (VIN = 0)	IIN	15	-	-0.1	-	-	µADC
	CIN	15	-	-	10	20	PF
Quiescent Current (AL Device) (Per Package)	IDD	5.0	1.0	0.002	1.0	1.0	µADC
	IDD	10	2.0	0.004	2.0	2.0	µADC
Quiescent Current (CL/CP Device) (Per Package)	IDD	5.0	4.0	0.002	4.0	4.0	µADC
	IDD	10	8.0	0.004	8.0	8.0	µADC
Total Supply Current * (Dynamic plus Quiescent, Per Package) (CL 50 pF on all outputs, all buffers switching)	IT	5.0	15	1.8 µA/kHz†	16	16	µADC
	IT	10	15	3.5 µA/kHz†	16	16	µADC

*Low = 55°C for AL Device, -40°C for CL/CP Device.
 †High = +125°C for AL Device, +85°C for CL/CP Device.
 ‡To Calculate total supply current at loads other than 50 pF:
 $I(T_{CL}) = I(150 \text{ pF}) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$
 where: I is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.
 *The formulas given are for the typical characteristics only at 25°C.

†Noise immunity specified for worst-case input combination
 ‡Suffix Noise Margin for both "...1" and "...0" level =
 1.0 Vdc min @ VDD = 5.0 Vdc
 2.0 Vdc min @ VDD = 10 Vdc
 2.5 Vdc min @ VDD = 15 Vdc
 UB Suffix Noise Margin for both "...1" and "...0" level =
 0.5 Vdc min @ VDD = 5.0 Vdc
 1.0 Vdc min @ VDD = 10 Vdc
 1.0 Vdc min @ VDD = 15 Vdc

MC14049UB • MC14050B

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

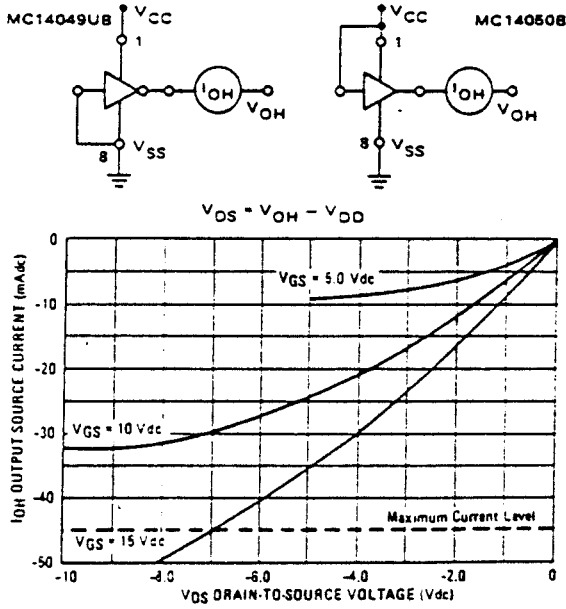


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

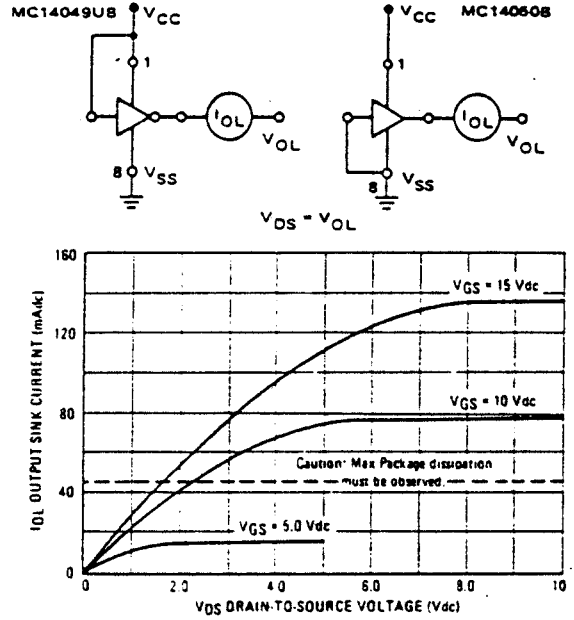
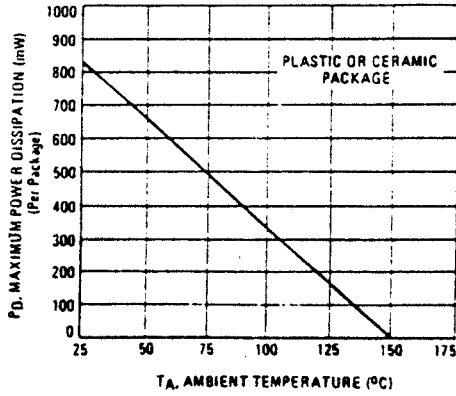
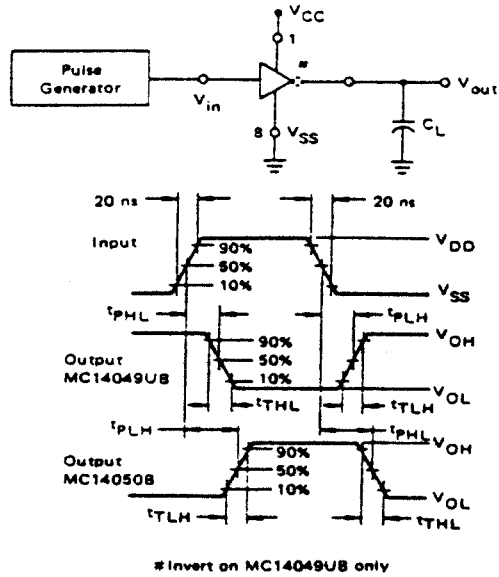


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



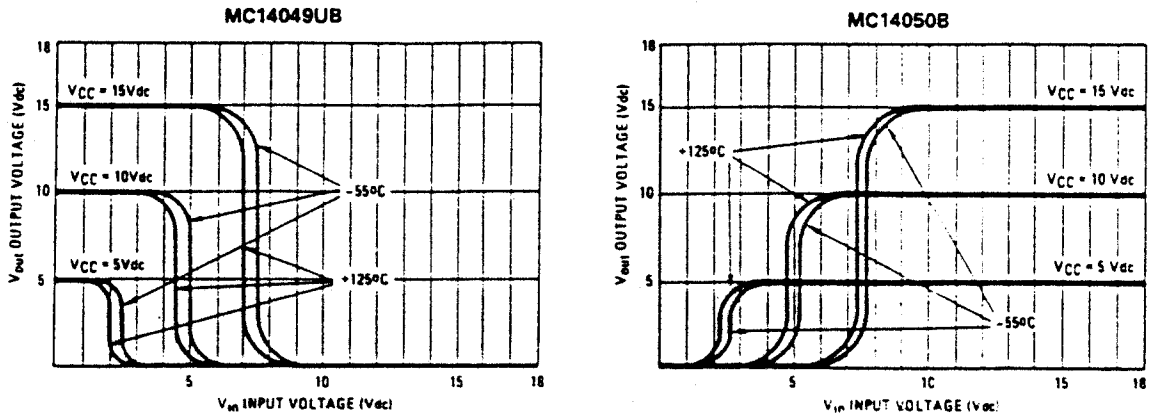
MC14049UB • MC14050B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ	Max	Unit
MC14049UB						
Output Rise Time $t_{TLH} = (0.8 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{TLH} = (0.27 \text{ ns/pF}) C_L + 26.5 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	160 100 60	ns
Output Fall Time $t_{THL} = (0.3 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.12 \text{ ns/pF}) C_L + 14 \text{ ns}$ $t_{THL} = (0.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{THL}	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.38 \text{ ns/pF}) C_L + 61 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH} = (0.11 \text{ ns/pF}) C_L + 24.5 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	80 40 30	120 65 50	ns
Propagation Delay Time $t_{PHL} = (0.38 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PHL} = (0.12 \text{ ns/pF}) C_L + 9 \text{ ns}$ $t_{PHL} = (0.11 \text{ ns/pF}) C_L + 4.5 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	30 15 10	60 30 20	ns
MC14050B						
Output Rise Time $t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	160 80 60	ns
Output Fall Time $t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$	t_{THL}	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$ $t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$ $t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	80 40 30	140 80 60	ns
Propagation Delay Time $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	40 20 15	80 40 30	ns

*The formulae given is for the typical characteristics only.

FIGURE 1 — TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



REPRODUCED COURTESY OF MOTOROLA, INC.

MC78L00C, AC Series

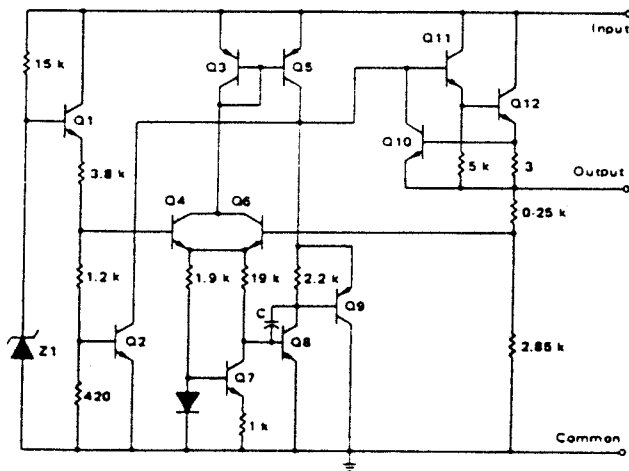
THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either $\pm 5\%$ (AC) or $\pm 10\%$ (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC

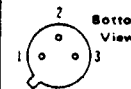


Device No. -10%	Device No. -5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

Pin 1. Output
2. Ground
3. Input

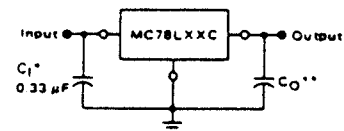


G SUFFIX
CASE 79
TO-39

Pin 1. Input
2. Output
3. Ground

(Case connected to pin 3)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_1 is required if regulator is located an appreciable distance from power supply filter.

** = C_2 is not needed for stability, however, it does improve transient response.

ORDERING INFORMATION

Device	Temperature Range	Package
MC78LXXACG	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC78LXXACP	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Transistor
MC78LXXCG	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC78LXXCP	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Transistor

XX indicates nominal voltage

MC78L00C, AC Series

MC78L00 Series MAXIMUM RATINGS ($T_A = +125^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V – 8.0 V) (12 V – 18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	0 to +150	$^\circ\text{C}$

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS ($V_I = 10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L05C			MC78L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	4.6	5.0	5.4	4.8	5.0	5.2	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $7.0\text{ Vdc} < V_I < 20\text{ Vdc}$ $8.0\text{ Vdc} < V_I < 20\text{ Vdc}$	Regline	–	55	200	–	55	150	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 40\text{ mA}$)	Regload	–	11	60	–	11	60	mV
Output Voltage ($7.0\text{ Vdc} < V_I < 20\text{ Vdc}$, $1.0\text{ mA} < I_O < 40\text{ mA}$) ($V_I = 10\text{ V}$, $1.0\text{ mA} < I_O < 70\text{ mA}$)	V_O	4.5 4.5	–	5.5 5.5	4.75 4.75	–	5.25 5.25	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	–	3.8	6.0	–	3.8	6.0	mA
Input Bias Current Change ($8.0\text{ Vdc} < V_I < 20\text{ Vdc}$) ($1.0\text{ mA} < I_O < 40\text{ mA}$)	$-I_{IB}$	–	–	1.5 0.2	–	–	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} < f < 100\text{ kHz}$)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $8.0\text{ V} < V_I < 18\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L00C, AC Series

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS ($V_I = 14\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L08C			MC78L08AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.36	8.0	8.64	7.7	8.0	8.3	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $10.5\text{ Vdc} < V_I < 23\text{ Vdc}$ $11\text{ Vdc} < V_I < 23\text{ Vdc}$	Regline	-	20	200	-	20	175	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 40\text{ mA}$)	Regload	-	15	80	-	15	80	mV
Output Voltage ($10.5\text{ Vdc} < V_I < 23\text{ Vdc}$, $1.0\text{ mA} < I_O < 40\text{ mA}$) ($V_I = 14\text{ V}$, $1.0\text{ mA} < I_O < 70\text{ mA}$)	V_O	7.2	-	8.8	7.6	-	8.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	-	3.0	6.0	-	3.0	6.0	mA
Input Bias Current Change ($11\text{ Vdc} < V_I < 23\text{ Vdc}$) ($1.0\text{ mA} < I_O < 40\text{ mA}$)	ΔI_{IB}	-	-	1.5	-	-	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} < f < 100\text{ kHz}$)	V_N	-	52	-	-	60	-	μV
Long-Term Stability	$\Delta V_O/\Delta t$	-	20	-	-	20	-	mV/10 k Hrs
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $12\text{ V} < V_I < 23\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	36	55	-	37	57	-	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	-	1.7	-	-	1.7	-	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS ($V_I = 19\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L12C			MC78L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.1	12	12.9	11.5	12	12.5	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $14.5\text{ Vdc} < V_I < 27\text{ Vdc}$ $16\text{ Vdc} < V_I < 27\text{ Vdc}$	Regline	-	120	250	-	120	250	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 40\text{ mA}$)	Regload	-	20	100	-	20	100	mV
Output Voltage ($14.5\text{ Vdc} < V_I < 27\text{ Vdc}$, $1.0\text{ mA} < I_O < 40\text{ mA}$) ($V_I = 19\text{ V}$, $1.0\text{ mA} < I_O < 70\text{ mA}$)	V_O	10.8	-	13.2	11.4	-	12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	-	4.2	6.5	-	4.2	6.5	mA
Input Bias Current Change ($16\text{ Vdc} < V_I < 27\text{ Vdc}$) ($1.0\text{ mA} < I_O < 40\text{ mA}$)	ΔI_{IB}	-	-	1.5	-	-	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} < f < 100\text{ kHz}$)	V_N	-	80	-	-	80	-	μV
Long-Term Stability	V_O/t	-	24	-	-	24	-	mV/10 k Hrs
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $15\text{ V} < V_I < 25\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	36	42	-	37	42	-	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	-	1.7	-	-	1.7	-	Vdc

MC78L00C, AC Series

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS ($V_I = 33\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L24C			MC78L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	22.1	24	25.9	23	24	25	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 27.5 Vdc $< V_I < 38\text{ Vdc}$ 28 Vdc $< V_I < 38\text{ Vdc}$ 27 Vdc $< V_I < 38\text{ Vdc}$	Reg _{line}	-	35	350	-	-	-	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 40\text{ mA}$)	Reg _{load}	-	40	200	-	40	200	mV
Output Voltage (28 Vdc $< V_I < 38\text{ Vdc}$, $1.0\text{ mA} < I_O < 40\text{ mA}$) (27 Vdc $< V_I < 38\text{ Vdc}$, $1.0\text{ mA} < I_O < 40\text{ mA}$) (28 Vdc $< V_I < 33\text{ V}$, $1.0\text{ mA} < I_O < 70\text{ mA}$) (27 Vdc $< V_I < 33\text{ V}$, $1.0\text{ mA} < I_O < 70\text{ mA}$)	V_O	21.6	-	26.4	22.8	-	25.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	-	3.1	6.5	-	3.1	6.5	mA
Input Bias Current Change (28 Vdc $< V_I < 38\text{ Vdc}$) (1.0 mA $< I_O < 40\text{ mA}$)	ΔI_{IB}	-	-	1.5	-	-	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $< f < 100\text{ kHz}$)	V_N	-	200	-	-	200	-	μV
Long-Term Stability	$\Delta V_O/\text{yr}$	-	56	-	-	56	-	mV/1.0 k Hrs
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, 29 V $< V_I < 35\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	30	43	-	31	45	-	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	-	1.7	-	-	1.7	-	Vdc

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation

$$P_{D(T_A)} = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}(\text{Typ})} \geq V_I I_S - V_O I_O$$

Where $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

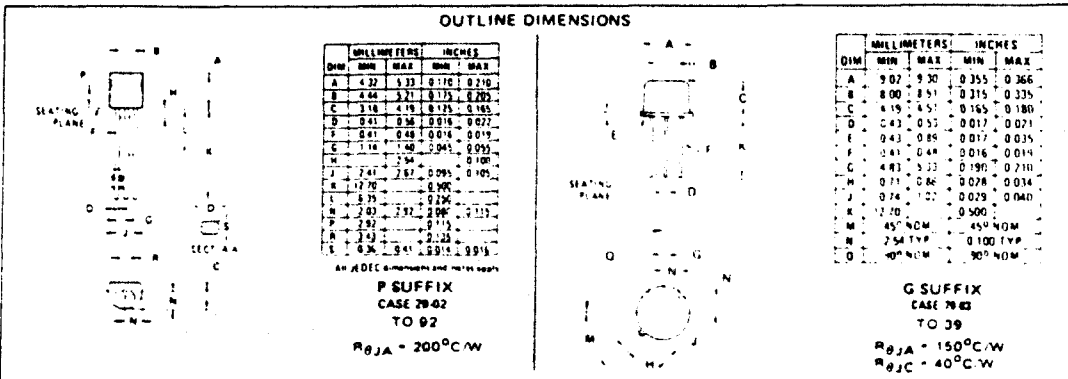
$T_{J(\text{max})}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(\text{Typ})$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

OUTLINE DIMENSIONS



MC78L00C, AC Series

TYPICAL CHARACTERISTICS ($T_A = -25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 - DROPOUT CHARACTERISTICS

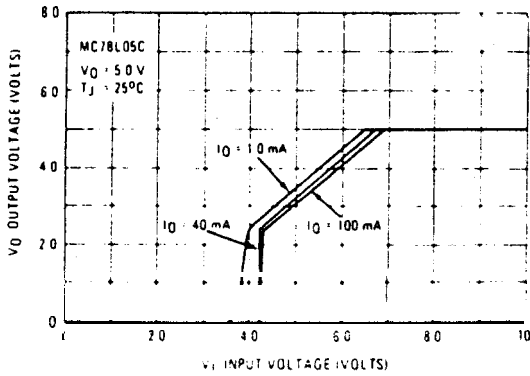


FIGURE 2 - DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

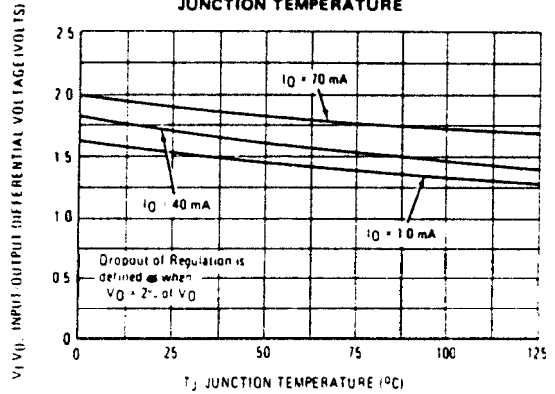


FIGURE 3 - INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

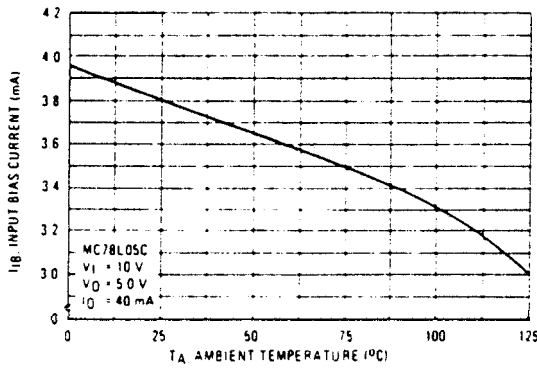


FIGURE 4 - INPUT BIAS CURRENT versus INPUT VOLTAGE

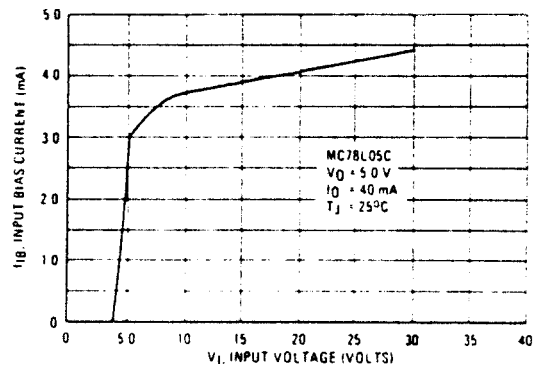


FIGURE 5 - MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE - TO-92 Type Package

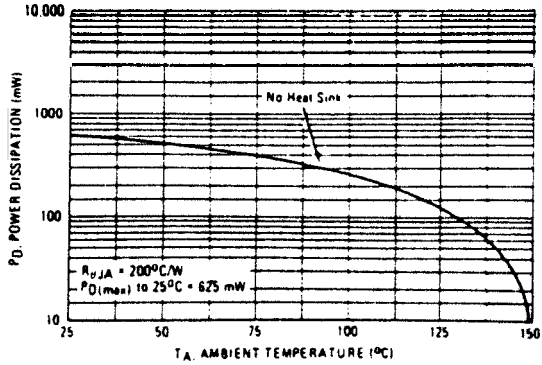
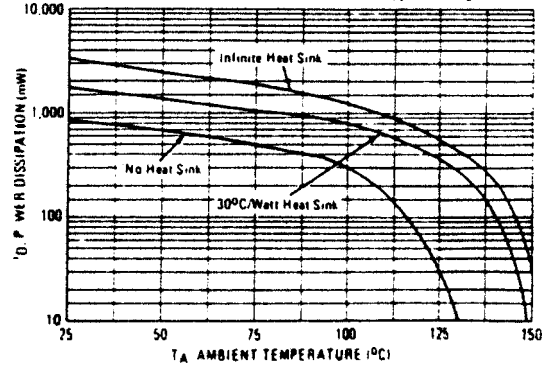


FIGURE 6 - MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE - TO-39 Type Package



MC78L00C, AC Series

APPLICATIONS INFORMATION

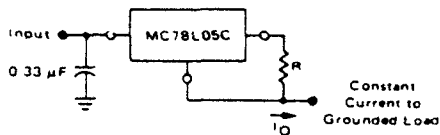
Design Considerations

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be

selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μ F or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 - CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5 \text{ V}}{R} + I_{18}$$

$I_{18} = 3.8 \text{ mA}$ over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts

FIGURE 8 - ±15 V TRACKING VOLTAGE REGULATOR

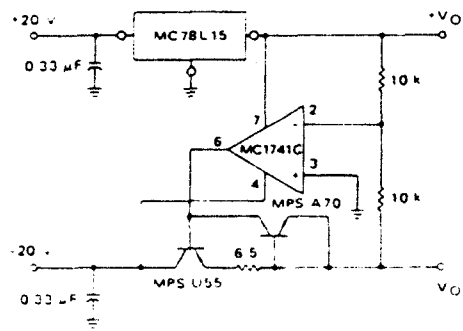
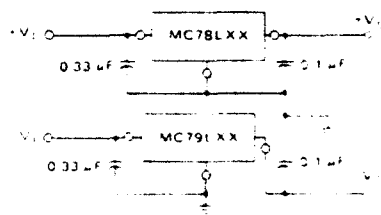
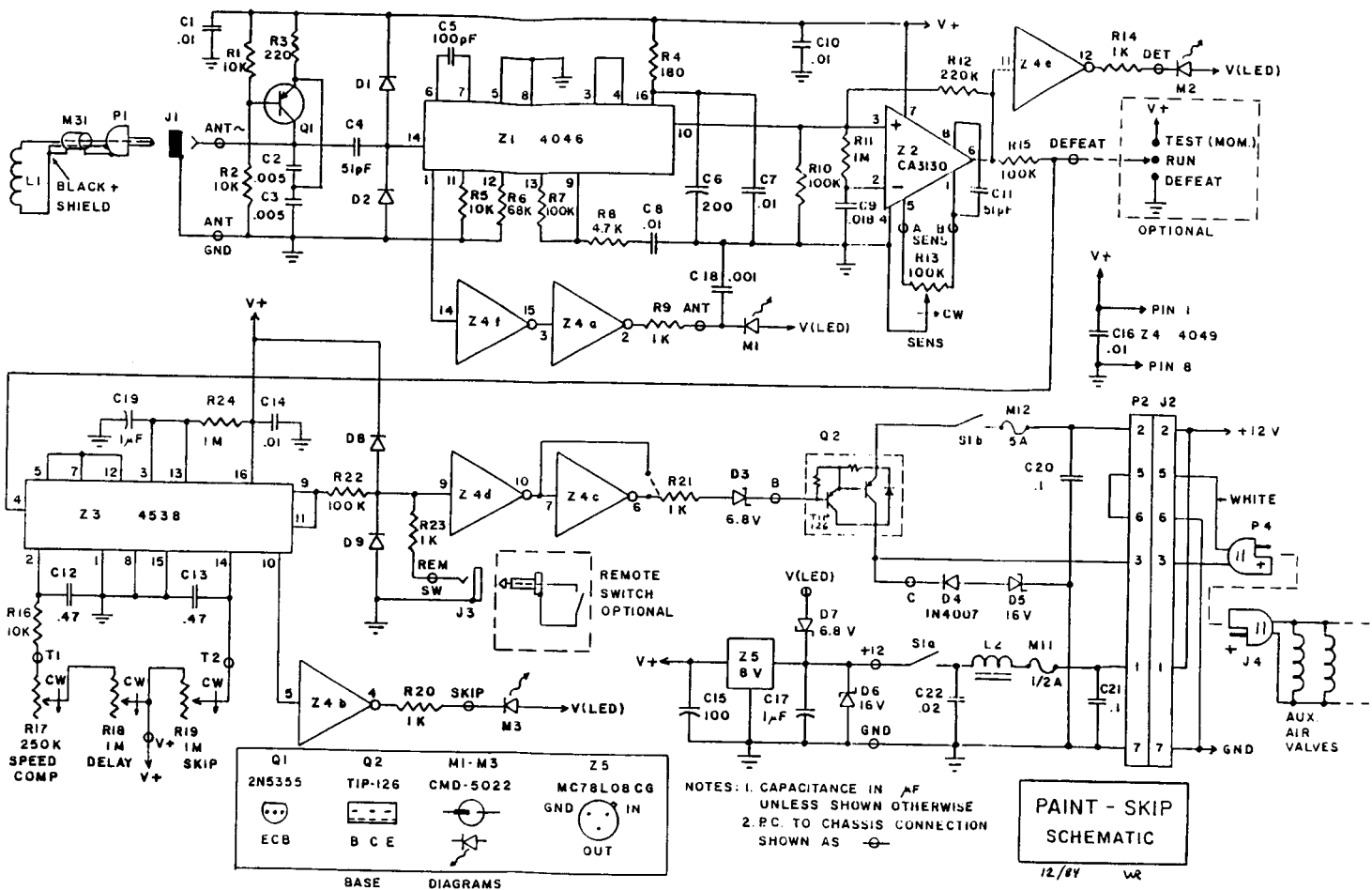


FIGURE 9 - POSITIVE AND NEGATIVE REGULATOR





Q1	Q2	M1-M3	Z5
2N5355	TIP-126	CMD-5022	MC78L08CG
ECB	B C E		GND IN OUT

BASE DIAGRAMS

NOTES: 1. CAPACITANCE IN μ F UNLESS SHOWN OTHERWISE
 2. P.C. TO CHASSIS CONNECTION SHOWN AS \ominus

PAINT - SKIP SCHEMATIC
 12/84 WR